Output Stages and Power Amplifiers

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Power BJTs

- Power transistors are large-area devices. Because of difference in geometry and doping concentrations, their properties tend to vary from those of the small-signal devices.
- The current gain of power BJTs is generally smaller in the range of 20 to 100, and may be a strong function of collector current and temperature.
- At high current levels, the current gain tends to drop off significantly, and parasitic resistances in the base and collector regions may become significant, affecting the transistor terminal characteristics.
- The maximum rated collector current $I_{C,\text{rated}}$
- The avalanche breakdown voltage (when the base is open) V_{CEO}
- The minimum voltage sustaining the transistor in breakdown $V_{CE(\text{sus})}$
- Second breakdown: permanent failure

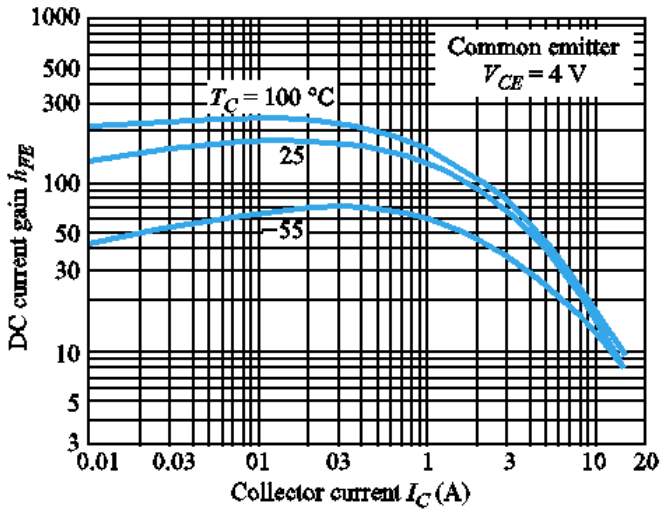


Figure 8.1 Typical dc beta characteristics (h_{FE} versus I_C) for 2N3055

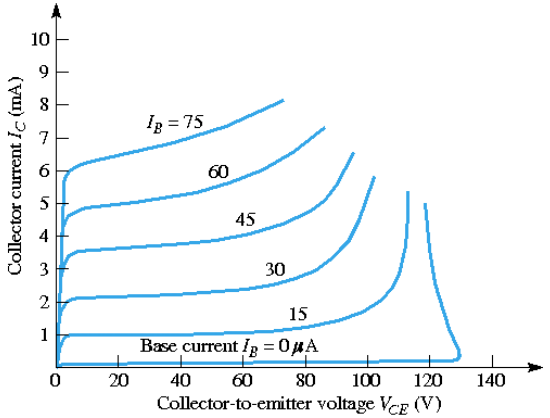


Figure 8.2 Typical collector current versus collector–emitter voltage characteristics of a bipolar transistor, showing breakdown effects

Safe Operating Area of BJTs

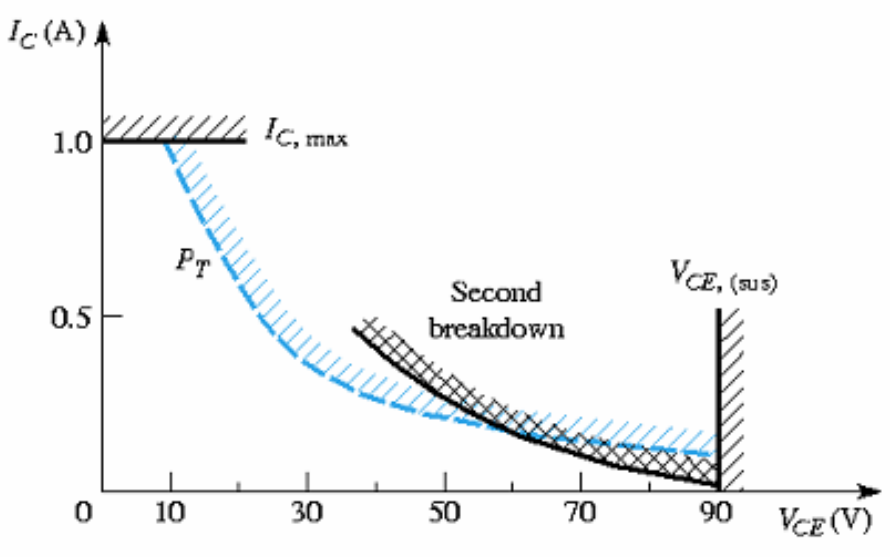
- The instantaneous and average power dissipation

$$p_Q = v_{CE} i_C + v_{BE} i_B \approx v_{CE} i_C$$

$$\overline{P}_Q = \frac{1}{T}\int_0^T v_{CE} i_C dt$$

- DC maximum rated power

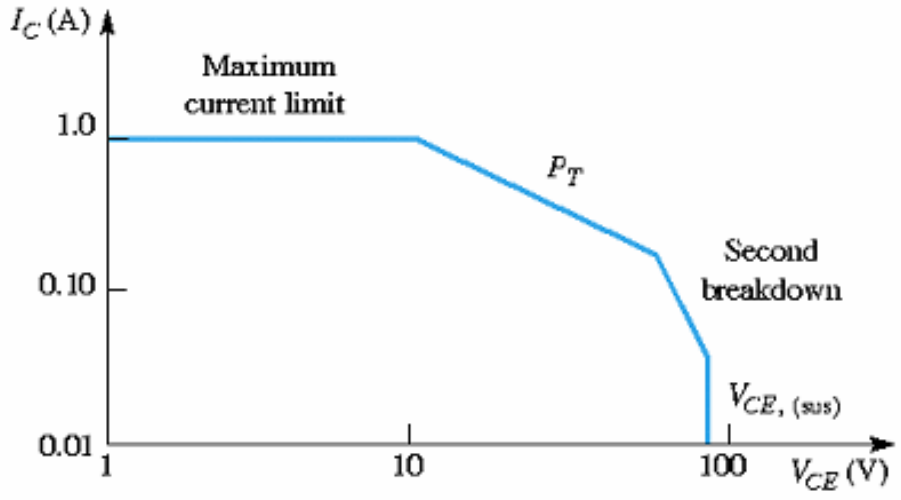
$$P_T = V_{CE} I_C$$



- Safe Operating Area (SOA): The region where the transistor can be operated safely.
  - ✓ SOA is bounded by

$$I_{C,\text{rated}},\ V_{CE(\text{sus})},\ P_T,$$

Second breakdown curve



Example 8.1 **Objective:** Determine the required current, voltage, and power ratings of a power BJT.

Consider the common-emitter circuit in Figure 8.4. The parameters are $R_L = 8\,\Omega$ and $V_{CC} = 24\,\text{V}$.

Solution: For $V_{CE} \approx 0$, the maximum collector current is

$$I_C(\text{max}) = \frac{V_{CC}}{R_L} = \frac{24}{8} = 3\,\text{A}$$

For $I_C = 0$, the maximum collector–emitter voltage is

$$V_{CE}(\text{max}) = V_{CC} = 24\,\text{V}$$

The load line is given by

$$V_{CE} = V_{CC} - I_C R_L$$

and must remain within the safe operating area, as shown in Figure 8.5.

The transistor power dissipation is therefore

$$P_T = V_{CE} I_C = (V_{CC} - I_C R_L) I_C = V_{CC} I_C - I_C^2 R_L$$

The current at which the maximum power occurs is found by setting the derivative of this equation equal to zero as follows:

$$\frac{dP_T}{dI_C} = 0 = V_{CC} - 2 I_C R_L$$

which yields

$$I_C = \frac{V_{CC}}{2R_L} = \frac{24}{2(8)} = 1.5\,\text{A}$$

The C–E voltage at the maximum power point is

$$V_{CE} = V_{CC} - I_C R_L = 24 - (1.5)(8) = 12\,\text{V}$$

The maximum power dissipation in the transistor occurs at the center of the load line. The maximum transistor power dissipation is therefore

$$P_T = V_{CE} I_C = 12(1.5) = 18\,\text{W}$$

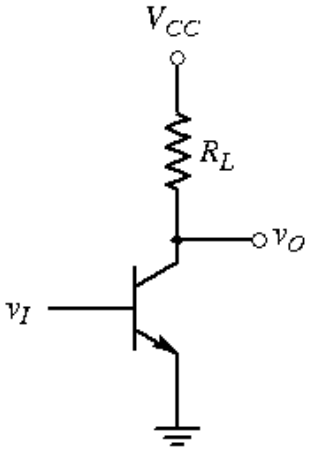
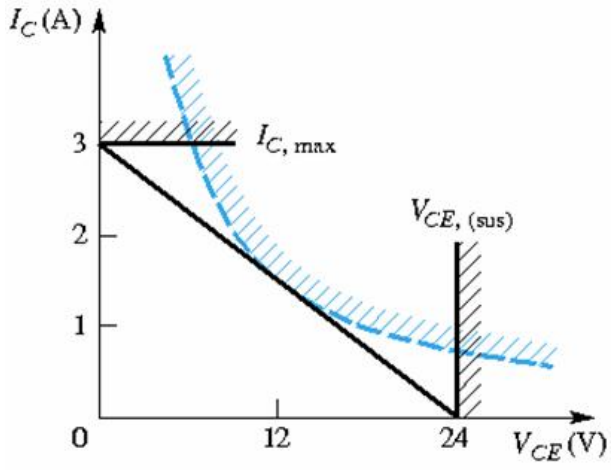


Figure 8.4 Figure for Example 8.1



Power MOSFETs

- The superior performance characteristics of power MOSFETs
  - ✓ Faster switching times
  - ✓ No second breakdown
  - ✓ Stable gain and response over a wide temperature range

- A MOSFET is a high impedance, voltage-controlled device, the drive circuitry is simpler.
  - ✓ The gate of a 10A power MOSFET may be driven by the output of a standard logic circuit.
  - ✓ In contrast, if the current gain of a 10A BJT is $\beta = 10$, then a base current of 1A is required for a collector current of 10A.

Heat Sinks

- The power dissipated in a transistor increases its internal temperature above the ambient temperature.
- If the device or junction temperature becomes too high, the transistor may suffer permanent damage.
- Special precautions must be taken in packaging power transistors and in providing heat sinks so that heat can be conducted from the transistor.

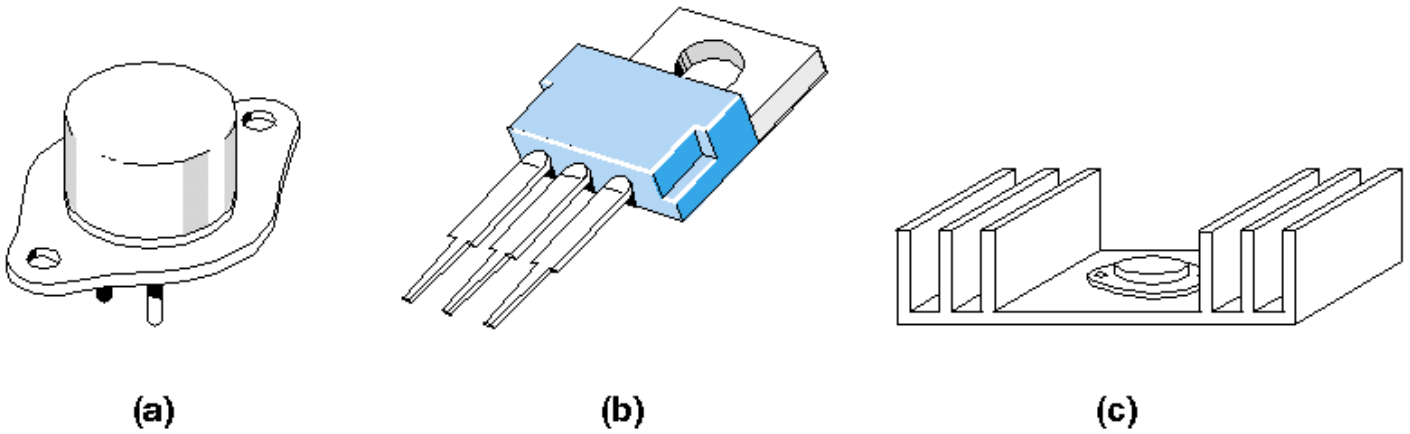


Figure 8.10 Two packaging schemes: (a) and (b) for power transistors and (c) typical heat sink

Thermal Resistance

- The temperature difference across an element with a thermal resistance θ is

$$T_2 - T_1 = P\theta$$

P: thermal power through the element

- Electrical equivalent circuit for heat flow from the device to the ambient

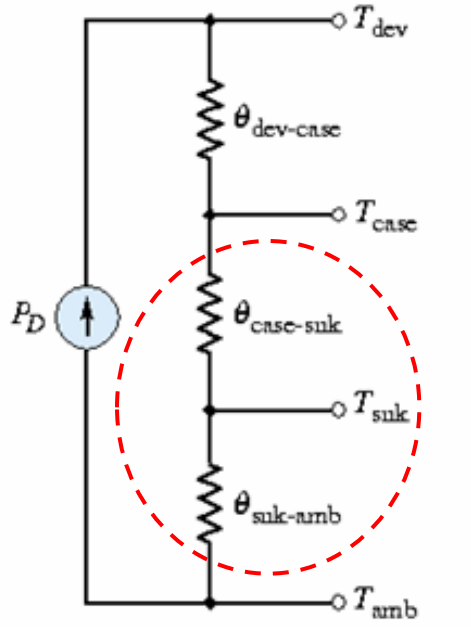


Figure 8.11 Electrical equivalent circuit for heat flow from the device to the ambient

When a heat sink is used:

$$T_{dev} - T_{amb} = P_D(\theta_{dev\text{-}case} + \theta_{case\text{-}sink} + \theta_{sink\text{-}amb})$$

When a heat sink is not used:

$$T_{dev} - T_{amb} = P_D(\theta_{dev\text{-}case} + \theta_{case\text{-}amb})$$

Example 8.2 **Objective:** Determine the maximum power dissipation in a transistor. Consider a power MOSFET for which the thermal resistance parameters are:

$$\theta_{\text{dev-case}} = 1.75\,^{\circ}\text{C/W} \qquad \theta_{\text{case-snk}} = 1\,^{\circ}\text{C/W}$$

$$\theta_{\text{snk-amb}} = 5\,^{\circ}\text{C/W} \qquad \theta_{\text{case-amb}} = 50\,^{\circ}\text{C/W}$$

The ambient temperature is $T_{\text{amb}} = 30\,^{\circ}\text{C}$, and the maximum junction or device temperature is $T_{j,\text{max}} = T_{\text{dev}} = 150\,^{\circ}\text{C}$.

Solution: When no heat sink is used, the maximum device power dissipation is found from Equation (8.7) as

$$P_{D,\text{max}} = \frac{T_{j,\text{max}} - T_{\text{amb}}}{\theta_{\text{dev-case}} + \theta_{\text{case-amb}}} = \frac{150 - 30}{1.75 + 50} = 2.32\,\text{W}$$

When a heat sink is used, the maximum device power dissipation is found from Equation (8.6) as

$$P_{D,\text{max}} = \frac{T_{j,\text{max}} - T_{\text{amb}}}{\theta_{\text{dev-case}} + \theta_{\text{case-snk}} + \theta_{\text{snk-amb}}} = \frac{150 - 30}{1.75 + 1 + 5} = 15.5\,\text{W}$$

Comment: These results illustrate that the use of a heat sink allows more power to be dissipated in the device, while keeping the device temperature at or below its maximum limit.

Classes of Power Amplifiers

- Power amplifiers are classified according to the percent of time the output transistors are conducting (turned on).
- Four principal classifications: class-A, class-B, class-AB, class-C

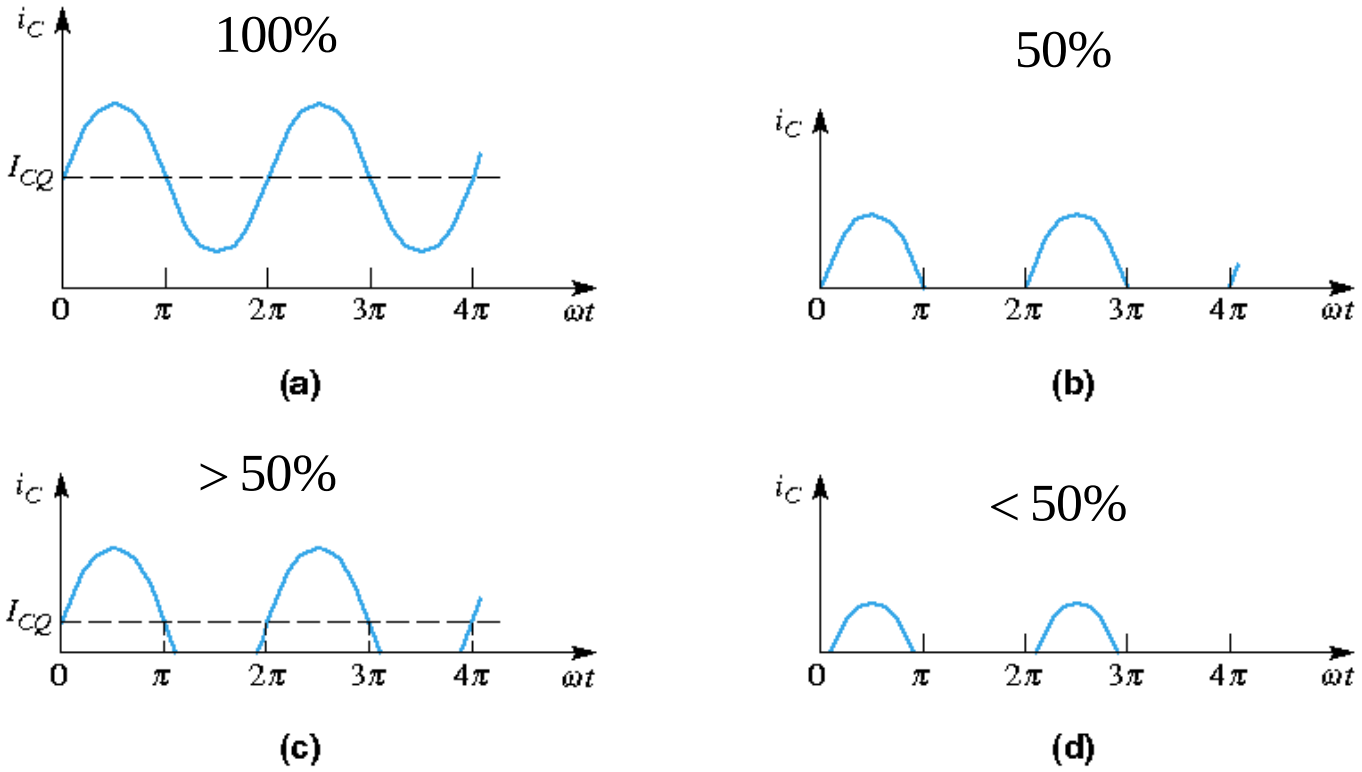


Figure 8.15 Collector current versus time characteristics: (a) class-A amplifier, (b) class-B amplifier, (c) class-AB amplifier, and (d) class-C amplifier

Class-A Operation

- Standard Class-A Amplifier

$$p_Q = v_{CE} i_C$$

$$i_C = I_{CQ} + I_{CQ} \sin \omega t$$

$$v_{CE} = \frac{V_{CC}}{2} - \frac{V_{CC}}{2} \sin \omega t$$

$$p_Q = v_{CE} i_C = \frac{V_{CC} I_{CQ}}{2} (1 - \sin^2 \omega t)$$

Load average ac power $\overline{P}_L = \frac{1}{2} \cdot \frac{V_{CC}}{2} \cdot I_{CQ} = \frac{V_{CC} I_{CQ}}{4}$

Power supply $\overline{P}_S = V_{CC} I_{CQ}$

Power Conversion Efficiency $\eta = \frac{\overline{P}_L}{\overline{P}_S} = 25\%$

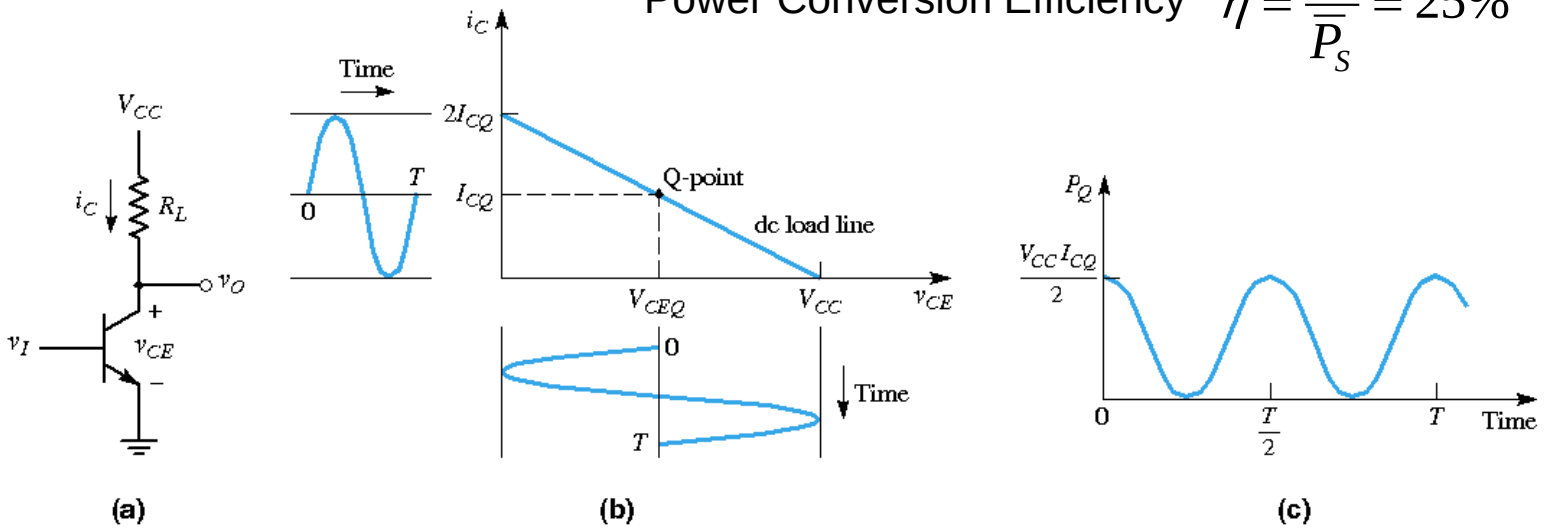
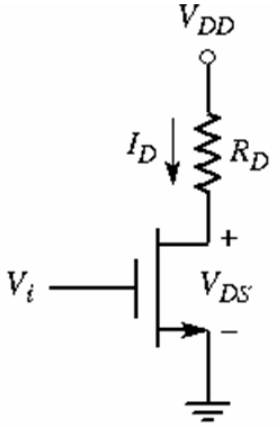


Figure 8.16 (a) Common-emitter amplifier, (b) dc load line, and (c) instantaneous power dissipation versus time in the transistor

Example 8.4 **Objective:** Calculate the actual efficiency of a class-A output stage.

Consider the common-source circuit in Figure 8.13. The circuit parameters are $V_{DD} = 10\,\text{V}$ and $R_D = 5\,\text{k}\Omega$, and the transistor parameters are: $K_n = 1\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0$. Assume the output voltage swing is limited to the range between the transition point and $v_{DS} = 9\,\text{V}$, to minimize nonlinear distortion.



Solution: The load line is given by

$$V_{DS} = V_{DD} - I_D R_D$$

At the transition point, we have

$$V_{DS}(\text{sat}) = V_{GS} - V_{TN}$$

and

$$I_D = K_n(V_{GS} - V_{TN})^2$$

Combining these expressions, the transition point is determined from

$$V_{DS}(\text{sat}) = V_{DD} - K_n R_D V_{DS}^2(\text{sat})$$

or

$$(1)(5)V_{DS}^2(\text{sat}) + V_{DS}(\text{sat}) - 10 = 0$$

which yields

$$V_{DS}(\text{sat}) = 1.32\,\text{V}$$

To obtain the maximum symmetrical swing under the conditions specified, we want the Q-point midway between $V_{DS} = 1.32\,\text{V}$ and $V_{DS} = 9\,\text{V}$, or

$$V_{DSQ} = 5.16\,\text{V}$$

The maximum ac component of voltage across the load resistor is then

$$v_r = 3.84 \sin \omega t$$

and the average power delivered to the load is

$$\overline{P}_L = \frac{1}{2} \cdot \frac{(3.84)^2}{5} = 1.47\,\text{mW}$$

The quiescent drain current is found to be

$$I_{DQ} = \frac{10 - 5.16}{5} = 0.968\,\text{mA}$$

The average power supplied by the V_{DD} source is

$$\overline{P}_S = V_{DD} I_{DQ} = (10)(0.968) = 9.68\,\text{mW}$$

and the power conversion efficiency, from Equation (8.12), is

$$\eta = \frac{\overline{P}_L}{\overline{P}_S} = \frac{1.47}{9.68} \Rightarrow 15.2\%$$

Class-B Operation

- Complementary Push-Pull Output Stage

1. $-0.6V < v_I < 0.6V$

   Qn: off, Qp: off

   $v_o = 0$

2. $v_I > 0.6V$

   Qn: on, Qp: off

   $v_o = v_I - 0.6$

3. $v_I < -0.6V$

   Qn: off, Qp: on

   $v_o = v_I + 0.6$

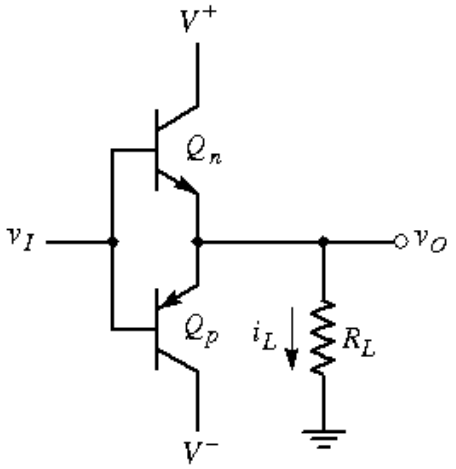


Figure 8.18 Basic complementary push–pull output stage

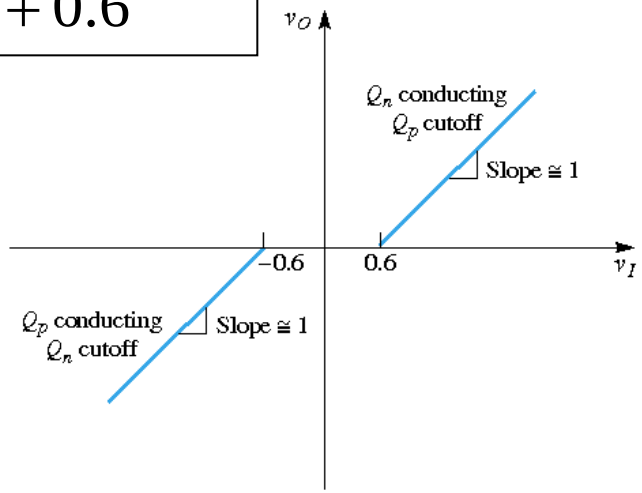


Figure 8.19 Voltage transfer characteristics of basic complementary push–pull output stage

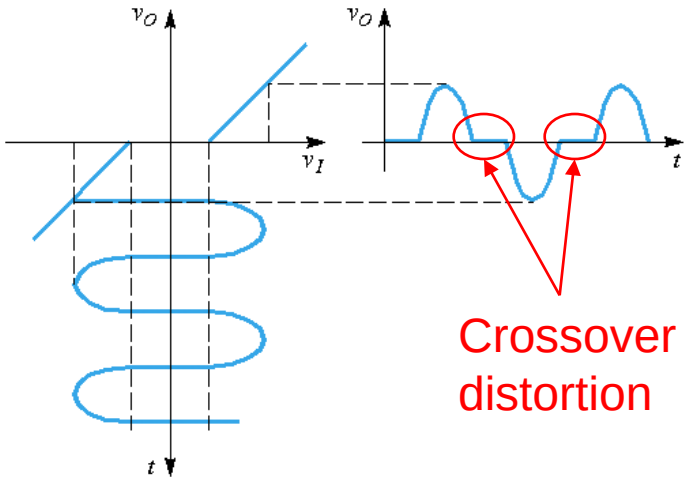


Figure 8.20 Crossover distortion of basic complementary push–pull output stage

Power Efficiency

For idealized class-B output stage,

$$v_O = V_P \sin \omega t$$

The instantaneous power dissipation in Qn is

$$p_{Qn} = v_{CEn} i_{Cn}$$

(1) $0 \le \omega t < \pi$,

$$i_{Cn} = \frac{v_O}{R_L} = \frac{V_p}{R_L} \sin \omega t$$

$$v_{CEn} = V_{CC} - V_p \sin \omega t$$

$$p_{Qn} = (V_{CC} - V_p \sin \omega t)\left(\frac{V_p}{R_L} \sin \omega t\right)$$

(2) $\pi \le \omega t < 2\pi$,

$$i_{Cn} = 0 \qquad p_{Qn} = 0$$

The average power dissipation in Qn is

$$\bar{p}_{Qn} = \frac{1}{2\pi} \int_0^{\pi} \left(\frac{V_{CC} V_p}{R_L} \sin \theta - \frac{V_p^2}{R_L} \sin^2 \theta \right) d\theta = \frac{V_{CC} V_p}{\pi R_L} - \frac{V_p^2}{4 R_L}$$

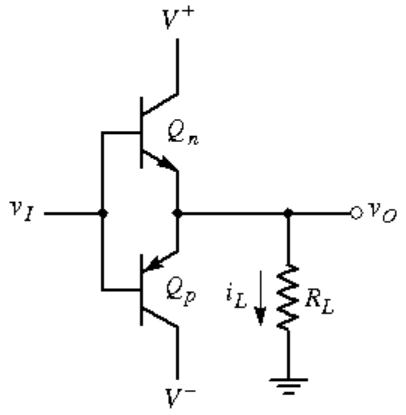


Figure 8.18 Basic complementary push–pull output stage

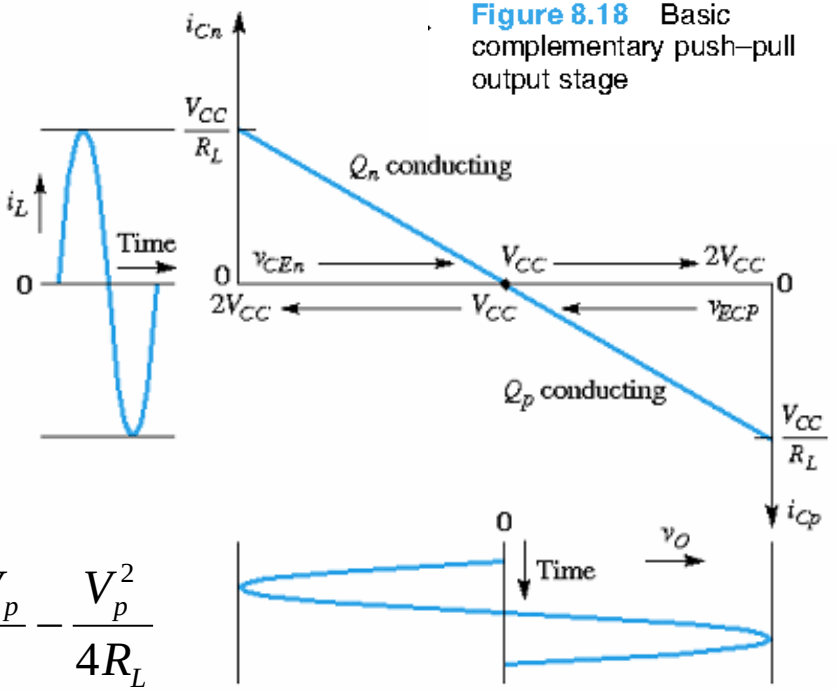


Figure 8.21 Effective load line of the class-B output stage

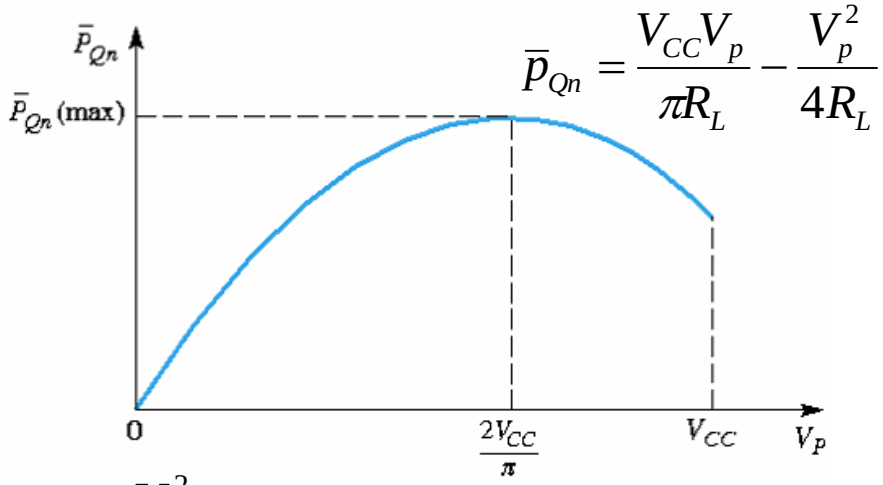
Power Efficiency

- Maximum average power dissipation

  setting the derivative of $\overline{p}_{Qn}$ with respect to Vp equal to zero,

$$\overline{p}_{Qn}(\max) = \frac{V_{CC}^2}{\pi^2 R_L}$$

$$V_{P|\overline{P}_{Qn}(\max)} = \frac{2V_{CC}}{\pi}$$



- Power conversion efficiency

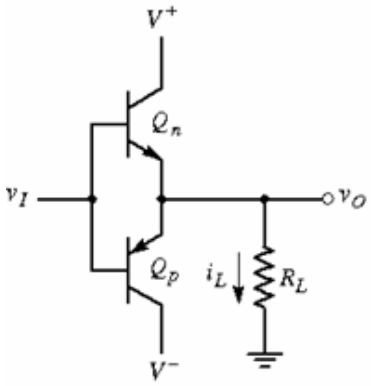
The average power delivered to the load $\overline{P}_L = \frac{1}{2}\frac{V_p^2}{R_L}$

The average current supplied by each source $\frac{1}{2\pi}\int_0^{\pi}\frac{V_p}{R_L}\sin\theta d\theta = \frac{V_p}{\pi R_L}$

The average current supplied by each source $\overline{P}_{V^+} = \overline{P}_{V^-} = \frac{V_{CC}V_p}{\pi R_L}$

The total average power $\overline{P}_S = \frac{2V_{CC}V_p}{\pi R_L}$

The conversion efficiency $\eta = \left(\frac{1}{2}\frac{V_p^2}{R_L}\right)\Big/\left(\frac{2V_{CC}V_p}{\pi R_L}\right) = \frac{\pi}{4}\frac{V_p}{V_{CC}}$



Maximum Conversion Efficiency

- Maximum Conversion Efficiency

$$\eta = \frac{\pi}{4}\frac{V_p}{V_{CC}}, \quad V_p \le V_{CC}$$

$$\eta(\max) = \frac{\pi}{4} = 78.5\%, \quad \text{when } V_p = V_{CC}$$

- Actual Conversion Efficiency: less than 78.5%
  - ✓ Circuit losses
  - ✓ Peak output voltage less than Vcc to avoid transistor saturation

- Conversion Efficiency when the maximum transistor power dissipation occurs

$$V_{P|\bar{P}_{Qn(\max)}} = \frac{2V_{CC}}{\pi}$$

$$\eta(\bar{P}_{Qn(\max)}) = \frac{\pi}{4}\frac{V_p}{V_{CC}} = \frac{\pi}{4}\frac{2V_{CC}/\pi}{V_{CC}} = 1/2 = 50\%$$

Class-AB Operation

- Class-AB output stage: applying a small quiescent bias on each output transistor to eliminate crossover distortion.

Let $v_I = 0, v_O = 0$, then $V_{BB}/2$ is applied to the B/E junction.

$$i_{Cn} = i_{Cp} = I_S e^{V_{BB}/2V_T}$$

(1) As v_I increases,

$$v_O = v_I + V_{BB}/2 - v_{BEn}$$

$$i_{Cn} = i_L + i_{Cp}$$

$$v_O \uparrow \Rightarrow i_L \uparrow \Rightarrow i_{Cn} \uparrow \Rightarrow v_{BEn} \uparrow \Rightarrow v_{EBp} \downarrow \Rightarrow i_{Cp} \downarrow$$

(2) As v_I goes negative,

$$v_O = v_I - V_{BB}/2 + v_{EBp}$$

$$v_O \downarrow \Rightarrow v_{EBp} \uparrow \Rightarrow i_{Cp} \uparrow \Rightarrow v_{BEn} \downarrow \Rightarrow i_{Cn} \downarrow$$

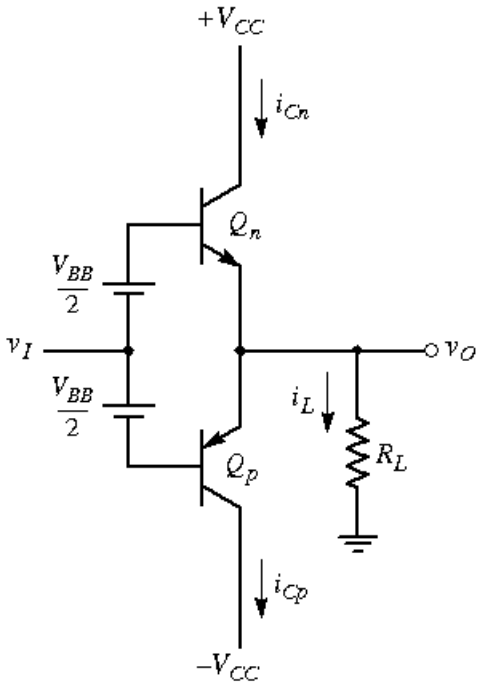


Figure 8.23 Bipolar class-AB output stage

Class-AB Operation

$$v_{BEn} + v_{EBp} = V_{BB}$$

$$V_T \ln\left(\frac{i_{Cn}}{I_S}\right) + V_T \ln\left(\frac{i_{Cp}}{I_S}\right) = 2V_T \ln\left(\frac{I_{CQ}}{I_S}\right)$$

I_{CQ} : quiescent collector current

$$i_{Cn} i_{Cp} = I_{CQ}^2$$

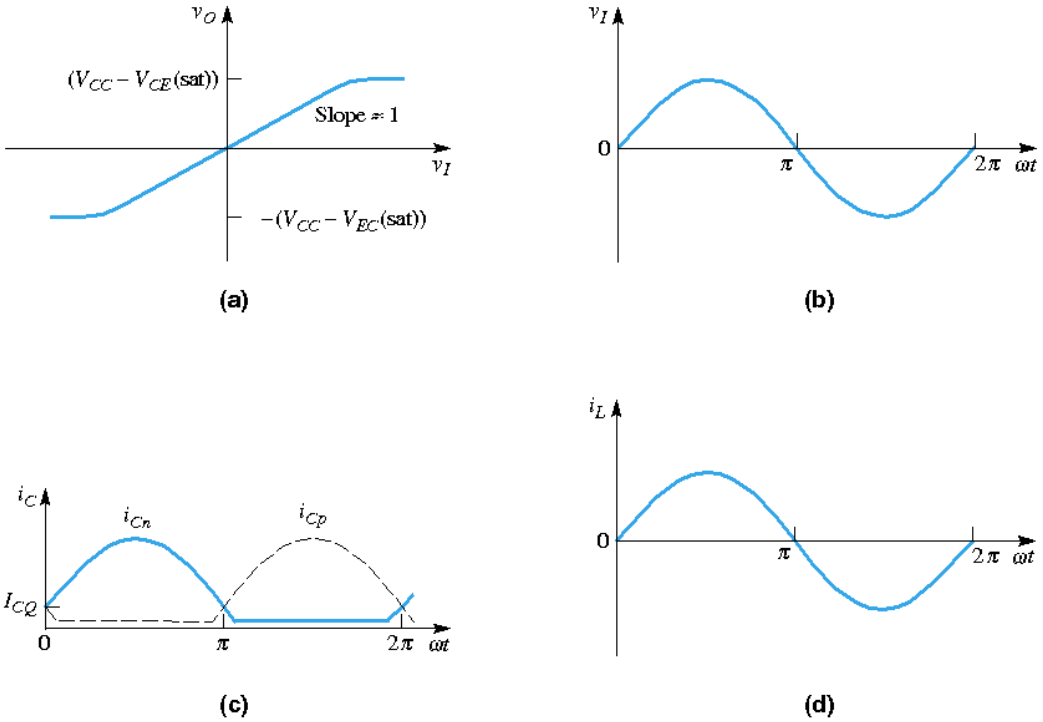


Figure 8.24 Characteristics of a class-AB output stage: (a) voltage transfer curve, (b) sinusoidal input signal, (c) collector currents, and (d) output current

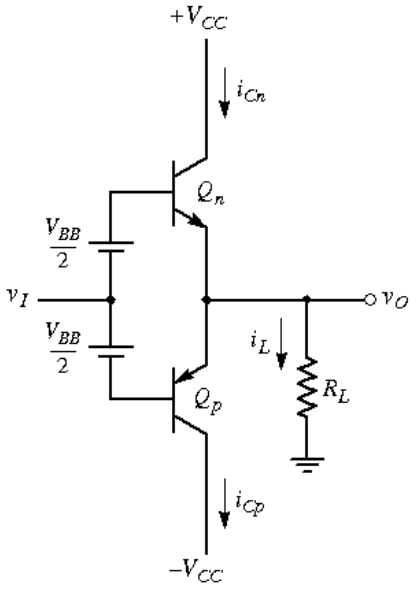


Figure 8.23 Bipolar class-AB output stage

Advantage of Class-AB Output Stages

- For a zero input signal, quiescent collector currents exist in the output transistors, the average power supplied by each source and the average power dissipated in each transistor are larger than for a class-B configuration.
  - ✓ Power conversion efficiency is less than for an idealized class-B circuit.

- The quiescent collector currents are usually small compared to the peak current, this increase in power dissipation is not great.

- The advantage of eliminating crossover distortion in the class-AB output stage greatly outweighs the slight disadvantage of reduced conversion efficiency and increased power dissipation.

Example 8.7 **Objective:** Determine the required biasing in a MOSFET class-AB output stage.

The circuit is shown in Figure 8.25. The parameters are $V_{DD} = 10\,\text{V}$ and $R_L = 20\,\Omega$. The transistors are matched, and the parameters are $K = 0.20\,\text{A/V}^2$ and $|V_T| = 1\,\text{V}$. The quiescent drain current is to be 20 percent of the load current when $v_O = 5\,\text{V}$.

Solution: For $v_O = 5\,\text{V}$,

$$i_L = 5/20 = 0.25\,\text{A}$$

Then, for $I_Q = 0.05\,\text{A}$ when $v_O = 0$, we have

$$I_{DQ} = 0.05 = K\left(\frac{V_{BB}}{2} - |V_T|\right)^2 = (0.20)\left(\frac{V_{BB}}{2} - 1\right)^2$$

which yields

$$V_{BB}/2 = 1.50\,\text{V}$$

The input voltage for v_O positive is

$$v_I = v_O + v_{GSn} - \frac{V_{BB}}{2}$$

For $v_O = 5\,\text{V}$ and $i_{Dn} \cong i_L = 0.25\,\text{A}$, we have

$$v_{GSn} = \sqrt{\frac{i_{Dn}}{K}} + |V_T| = \sqrt{\frac{0.25}{0.20}} + 1 = 2.12\,\text{V}$$

The source-to-gate voltage of M_p is

$$v_{SGp} = V_{BB} - V_{GSn} = 3 - 2.12 = 0.88\,\text{V}$$

which means that M_p is cut off and $i_{Dn} = i_L$. Finally, the input voltage is

$$v_I = 5 + 2.12 - 1.5 = 5.62\,\text{V}$$

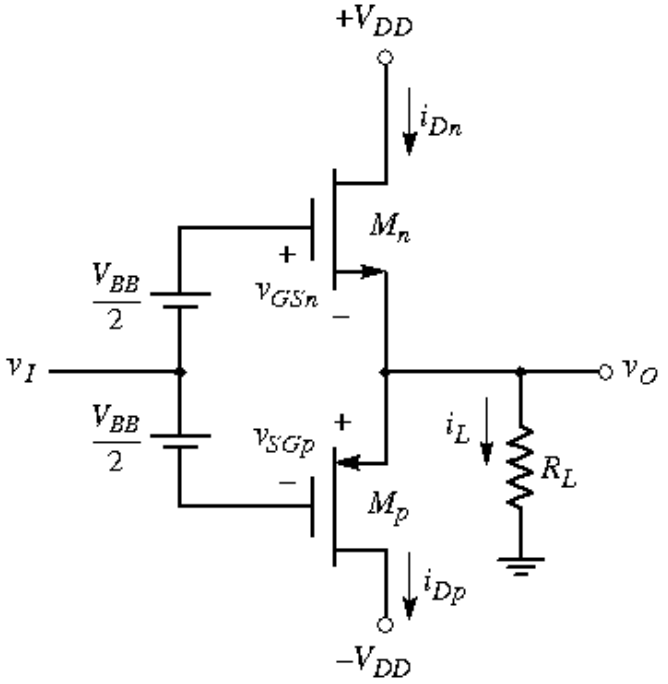


Figure 8.25 MOSFET class-AB output stage

Class-C Operation

- For class-C operation, the transistor has a reverse-biased BE voltage at the Q-point.
- The collector current is not negative, but is zero at the quiescent point.
- The transistor conducts for less than a half-cycle, which defines class-C operation.
- Conversion efficiency is large than 78.5% and usually used for RF circuits.

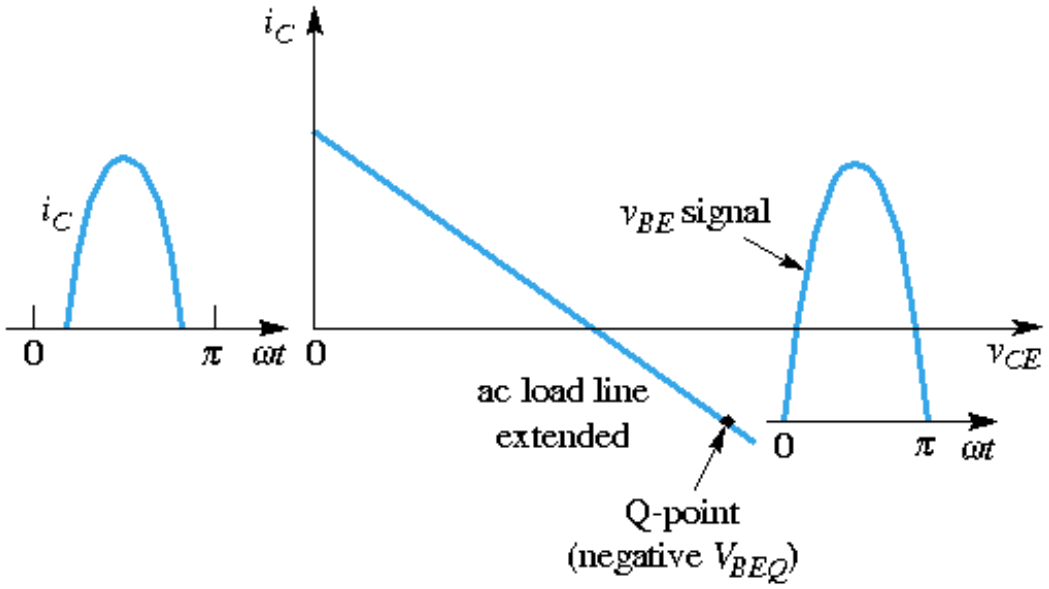


Figure 8.26 Effective ac load line of a class-C amplifier