The Field-Effect Transistor (FET)

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MOSFET

- The **metal-oxide-semiconductor field-effect transistor** (MOSFET) becomes a practical reality in the 1970s.
- The MOSFET, compared to BJTs, can be made very small, that is, it occupies a very small area in IC chip.
- In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current.
- The phenomenon applying an electric field perpendicular to the surface is called the **field effect**.
- Basic MOS capacitor structure

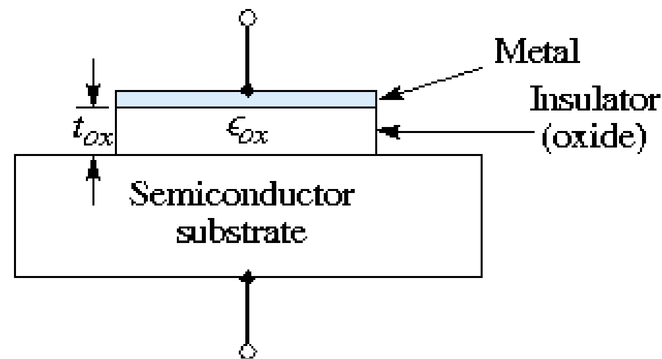


Figure 5.1 The basic MOS capacitor structure

The Physics of the MOS Capacitor

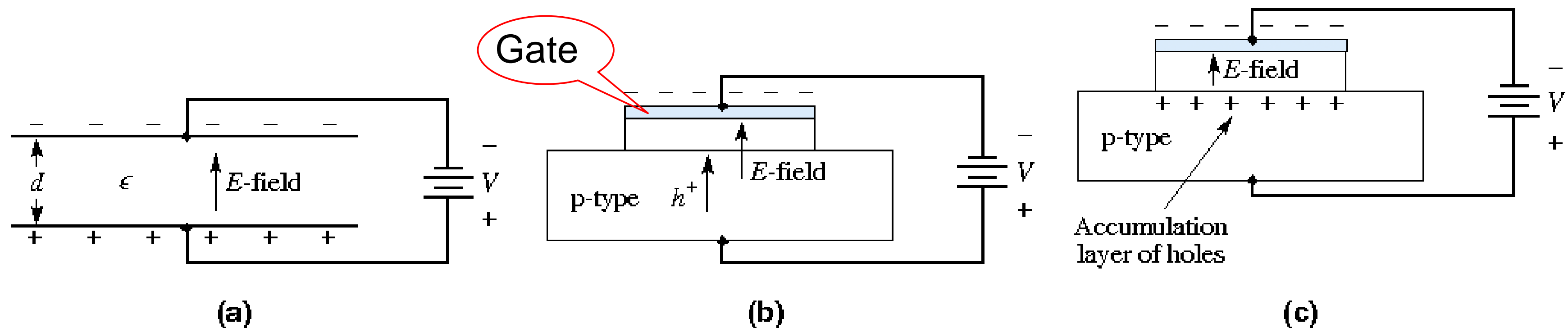


Figure 5.2 (a) A parallel-plate capacitor, showing the electric field and conductor charges, (b) a corresponding MOS capacitor with a negative gate bias, showing the electric field and charge flow, and (c) the MOS capacitor with an accumulation layer of holes

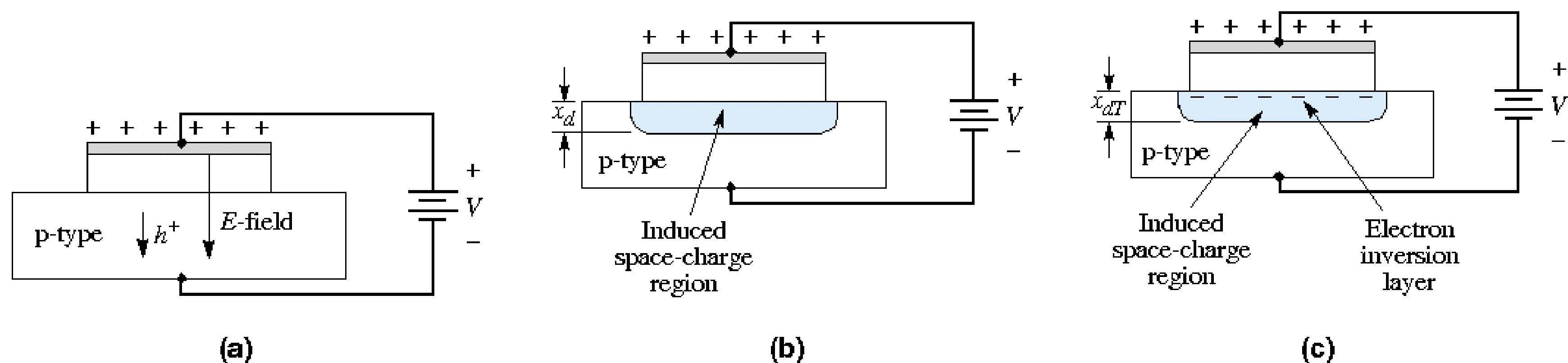


Figure 5.3 The MOS capacitor with p-type substrate: (a) effect of positive gate bias, showing the electric field and charge flow, (b) the MOS capacitor with an induced space-charge region due to a moderate gate bias, and (c) the MOS capacitor with an induced space-charge region and electron inversion layer due to a larger gate bias

The Physics of the MOS Capacitor for N-type Semiconductor Substrate

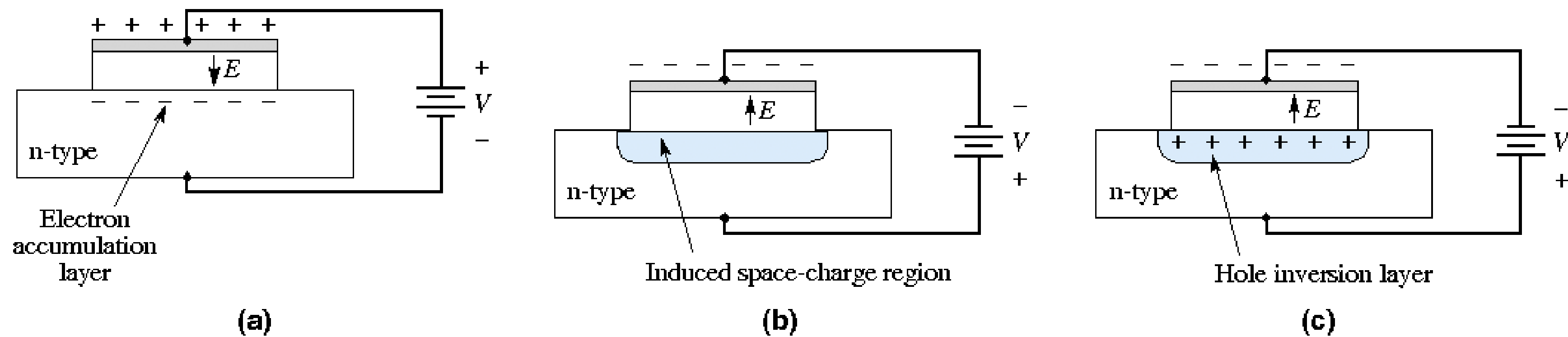


Figure 5.4 The MOS capacitor with n-type substrate for: (a) a positive gate bias, (b) a moderate negative bias, and (c) a larger negative bias

- Enhancement mode: a voltage must be applied to the gate to create an inversion layer.
  - ✓ P-type: a positive gate voltage must be applied to create the electron inversion layer
  - ✓ N-type: a negative gate voltage must be applied to create the hole inversion layer

NMOS

- Transistor Structure

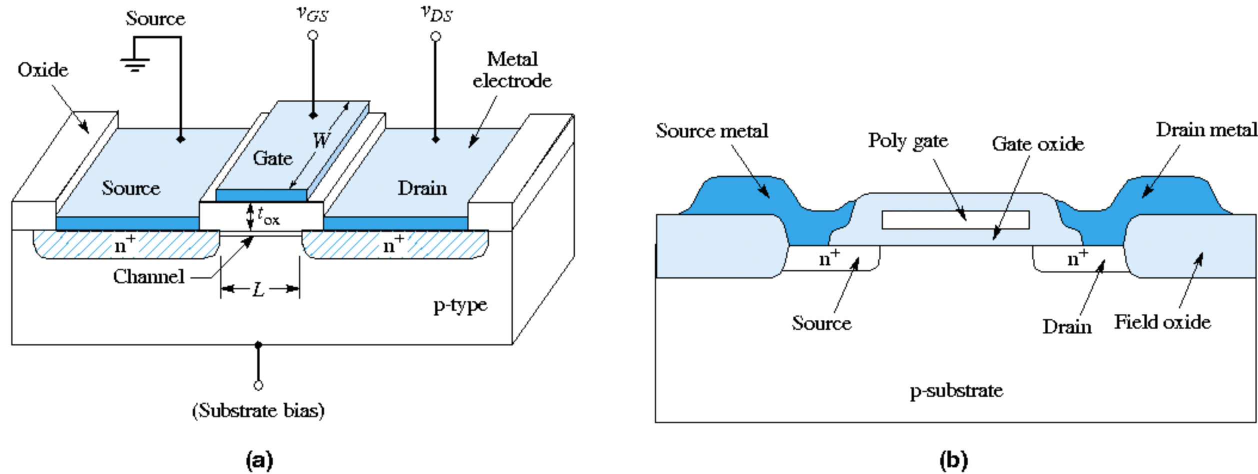
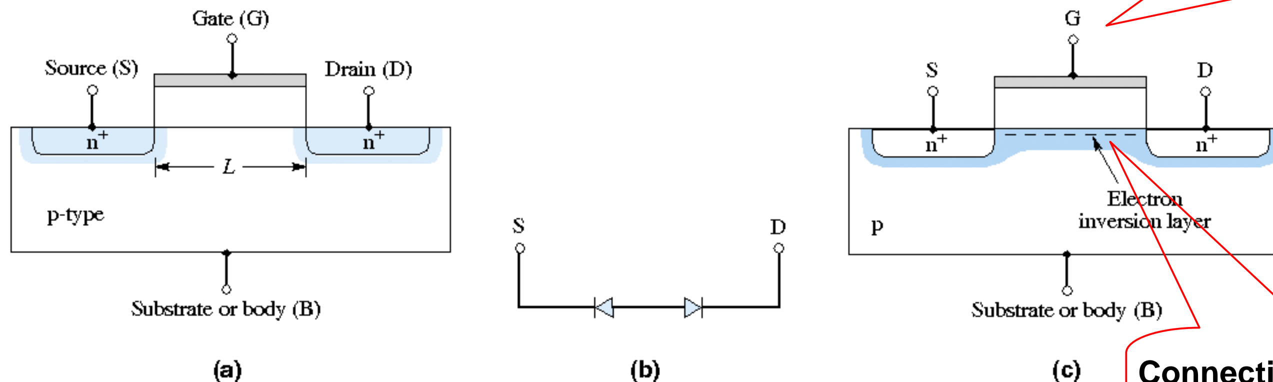


Figure 5.5 (a) Schematic diagram of an n-channel enhancement mode MOSFET and (b) an n-channel MOSFET, showing the field oxide and polysilicon gate

- Transistor Operation

Large enough positive voltage induces an electron inversion layer.



Connection between D and S is created so that a current can be generated.

Figure 5.6 (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

MOSFET Current-Voltage Characteristics

- The threshold voltage of the n-channel MOSFET is denoted as V_{TN} and is defined as the applied gate voltage needed to create an inversion charge.
- We can think of the threshold voltage as the gate voltage required to "turn on" the transistor.

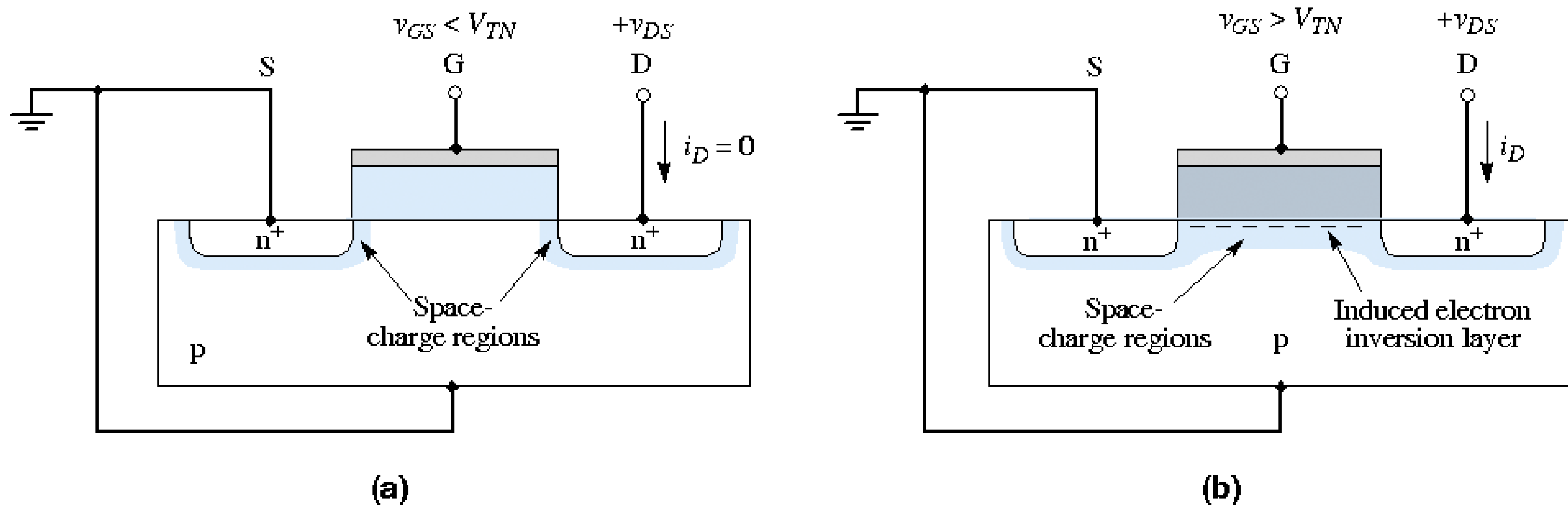


Figure 5.7 The n-channel enhancement-mode MOSFET (a) with an applied gate voltage $v_{GS} < V_{TN}$, and (b) with an applied gate voltage $v_{GS} > V_{TN}$

MOSFET Current-Voltage Characteristics

- The i_D versus v_{DS} characteristics for small values of v_{DS}

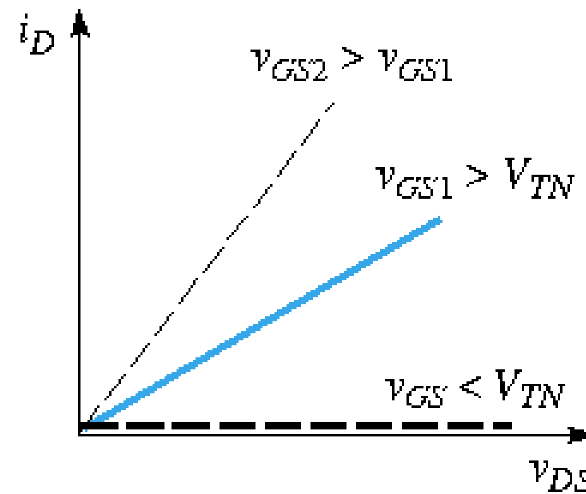


Figure 5.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS} at three v_{GS} voltages

MOSFET Current-Voltage Characteristics

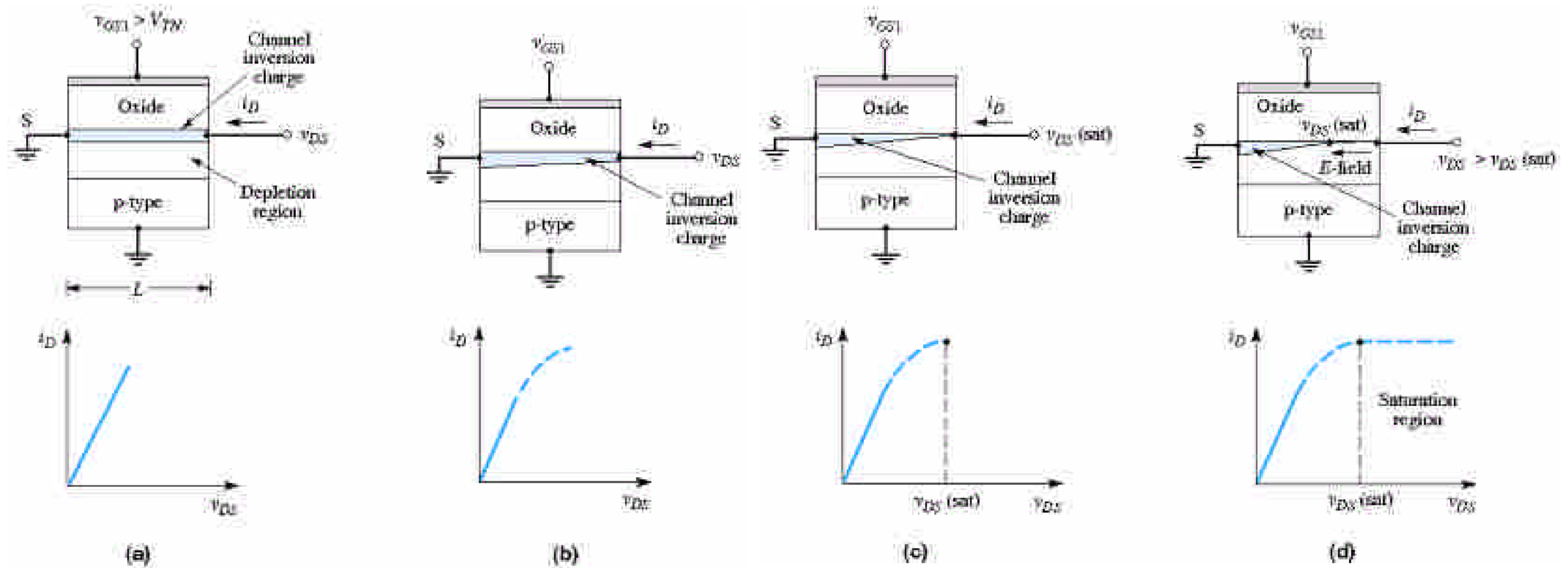


Figure 5.9 Cross section and i_D versus v_{DS} curve for an n-channel enhancement-mode MOSFET when $v_{GS} > V_{TN}$ for: (a) a small v_{DS} value, (b) a larger v_{DS} value, (c) $v_{DS} = v_{DS}(sat)$, and (d) $v_{DS} > v_{DS}(sat)$

Ideal MOSFET Current-Voltage Characteristics

- Nonsaturation (triode) Region

$$v_{DS} < v_{DS(sat)} = v_{GS} - V_{TN}$$

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] = K_n(2v_{DS(sat)}v_{DS} - v_{DS}^2)$$

- Saturation Region

$$v_{DS} > v_{DS(sat)} \quad (\text{also } v_{GS} > V_{TN})$$

$$i_D = K_n(v_{GS} - V_{TN})^2$$

Note: In the saturation region,

$$\frac{1}{r_o} = \partial i_D / \partial v_{DS} = \infty$$

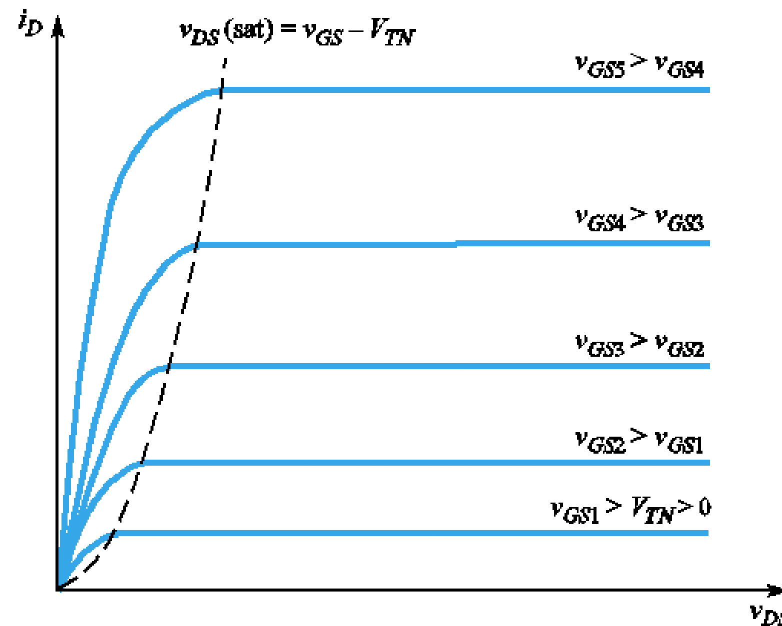


Figure 5.10 Family of i_D versus v_{DS} curves for an n-channel enhancement mode MOSFET

Conduction Parameter

- Conduction Parameter

$$K_n = \frac{W}{L} \cdot \frac{\mu_n C_{ox}}{2} \quad \text{(conduction parameter)}$$

C_{ox} : oxide capacitance per unit area $C_{ox} \propto \frac{1}{t_{ox}}, \quad t_{ox}$: oxide thickness

μ_n : electron mobility

W : channel width

L : channel length

- The conduction parameter is a function of both electrical and geometric parameters.
  - ✓ **Electrical Parameters**: The oxide capacitance and carrier mobility are essentially constants for a given technology.

$$K_n = \frac{W}{L} \cdot \frac{k'_n}{2} \qquad k'_n : \text{constant}$$

  - ✓ **Geometrical Parameters**: The width-to-length ratio (W/L) is a variable in the design of MOSFETs that is used to produce specific current-voltage characteritics in MOSFET circuits.

Example 5.1 **Objective:** Calculate the current in an n-channel MOSFET.

Consider an n-channel enhancement mode MOSFET with the following parameters: $V_{TN} = 0.75\,\text{V}$, $W = 40\,\mu\text{m}$, $L = 4\,\mu\text{m}$, $\mu_n = 650\,\text{cm}^2/\text{V–s}$, $t_{ox} = 450\,\text{Å}$, and $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})\,\text{F/cm}$. Determine the current when $V_{GS} = 2V_{TN}$, for the transistor biased in the saturation region.

Solution: The conduction parameter is determined by Equation (5.3(a)). First, consider the units involved in this equation, as follows:

$$K_n = \frac{W(\text{cm}) \cdot \mu_n\left(\dfrac{\text{cm}^2}{\text{V–s}}\right)\epsilon_{ox}\left(\dfrac{\text{F}}{\text{cm}}\right)}{2L(\text{cm}) \cdot t_{ox}(\text{cm})} = \frac{\text{F}}{\text{V–s}} = \frac{(\text{C/V})}{\text{V–s}} = \frac{\text{A}}{\text{V}^2}$$

The value of the conduction parameter is therefore

$$K_n = \frac{W\mu_n\epsilon_{ox}}{2Lt_{ox}} = \frac{(40 \times 10^{-4})(650)(3.9)(8.85 \times 10^{-14})}{2(4 \times 10^{-4})(450 \times 10^{-8})}$$

or

$$K_n = 0.249\,\text{mA/V}^2$$

From Equation (5.2(b)) for $v_{GS} = 2V_{TN}$, we find

$$i_D = K_n(v_{GS} - V_{TN})^2 = (0.249)(1.5 - 0.75)^2 = 0.140\,\text{mA}$$

Comment: The current capability of a transistor can be increased by increasing the conduction parameter. For a given fabrication technology, K_n is adjusted by varying the transistor width W.

PMOS

- In the p-channel enhancement-mode device, a negative gate-to-source voltage must be applied to create the inversion layer of holes that connects the source and drain regions.
- The threshold voltage, denoted an V_{TP} for the PMOS is negative for an enhancement-mode devices. The threshold voltage is positive for a depletion-mode device.
- Holes flow from the source to the drain, the conventional current enters the source and leaves the drain.

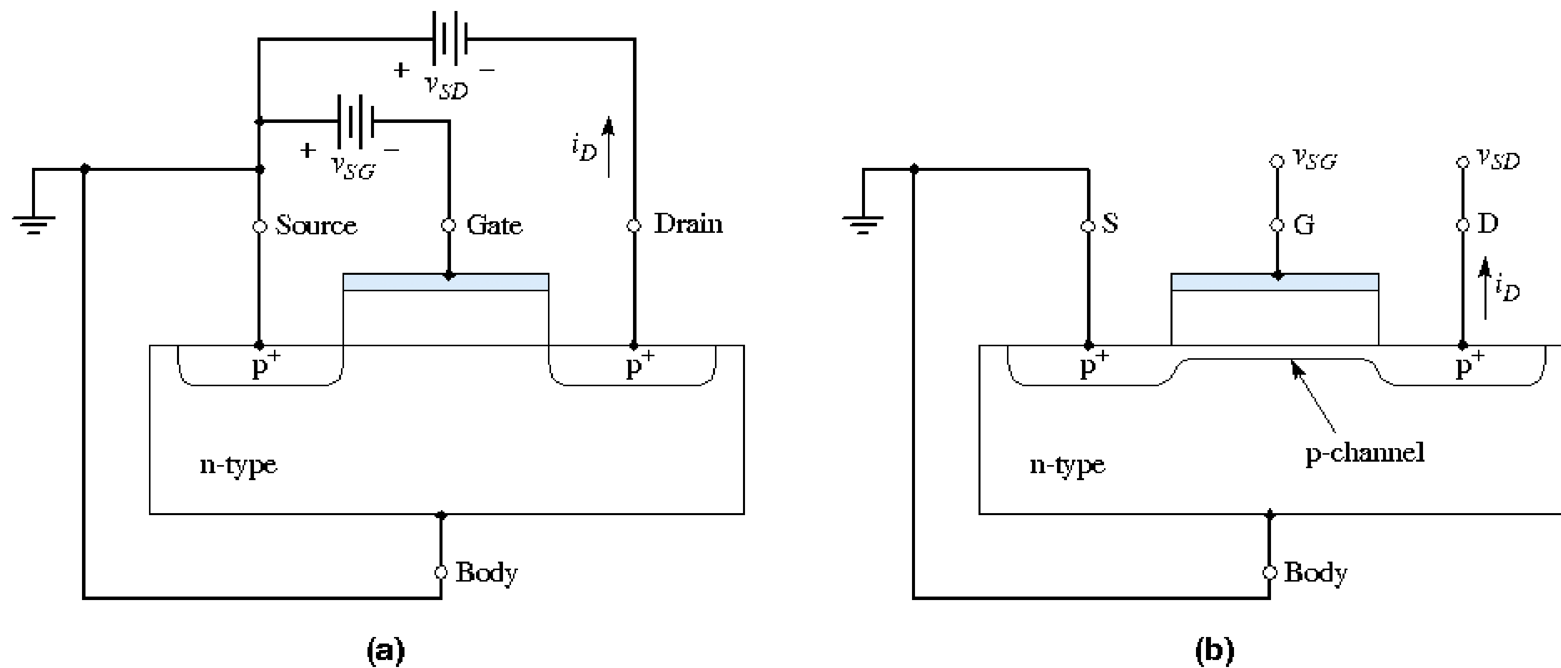


Figure 5.15 Cross section of p-channel MOSFETs: (a) enhancement-mode and (b) depletion-mode

Ideal PMOS Current-Voltage Relationship

- Nonsaturation (triode) Region

$$\text{when } v_{SD} < v_{SD(sat)} = v_{SG} + V_{TP}:$$

$$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2] = K_p(2v_{SD(sat)}v_{SD} - v_{SD}^2)$$

- Saturation Region

$$\text{when } v_{SD} > v_{SD(sat)} \quad (\text{also } v_{SG} + V_{TP} > 0): \quad i_D = K_p(v_{SG} + V_{TP})^2$$

Example 5.2 **Objective:** Determine the source-to-drain voltage required to bias a p-channel depletion-mode MOSFET in the saturation region.

Consider a depletion-mode p-channel MOSFET for which $K_p = 0.2\,\text{mA/V}^2$, $V_{TP} = +0.50\,\text{V}$, and $i_D = 0.50\,\text{mA}$.

Solution: In the saturation region, the drain current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2$$

or

$$0.50 = 0.2(v_{SG} + 0.50)^2$$

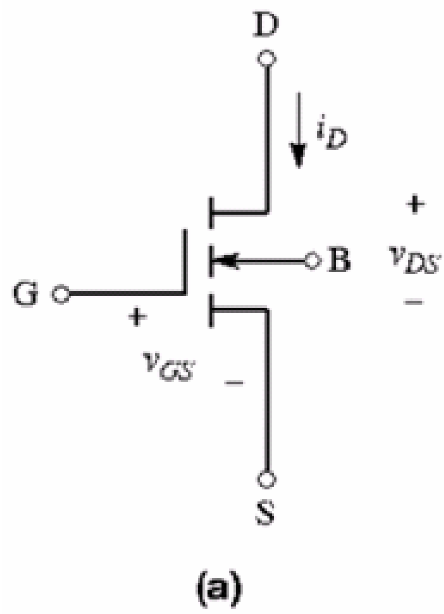
which yields

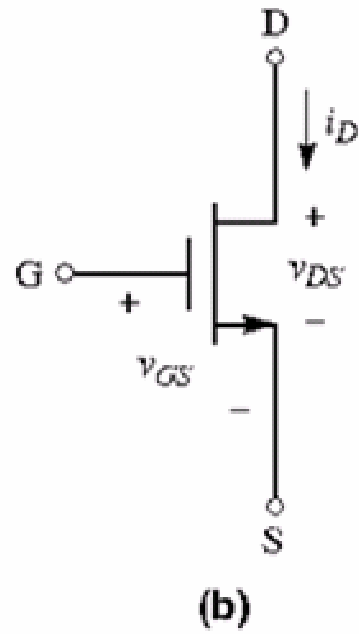
$$v_{SG} = 1.08\,\text{V}$$

To bias this p-channel MOSFET in the saturation region, the following must apply:

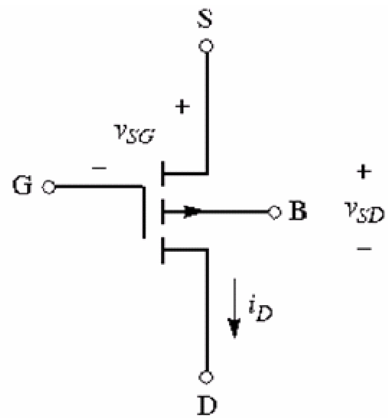
$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} = 1.08 + 0.5 = 1.58\,\text{V}$$

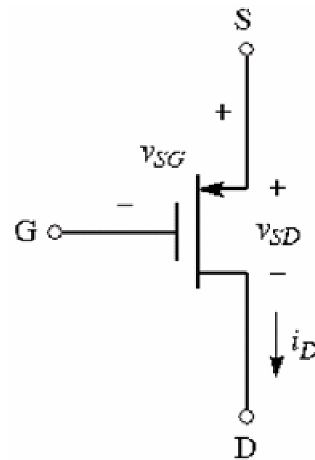
Circuit Symbols





N-channel enhancement-mode MOSFET





P-channel enhancement-mode MOSFET

Depletion-Mode MOSFET

- When zero volts are applied to the gate, an n-channel region (inversion layer) exists under the oxide of impurities introduced during device fabrication.
- The term **depletion mode** means that a channel exists even at zero gate voltage.
- A negative voltage must be applied to the n-channel depletion-mode MOSFET to turn the device off.

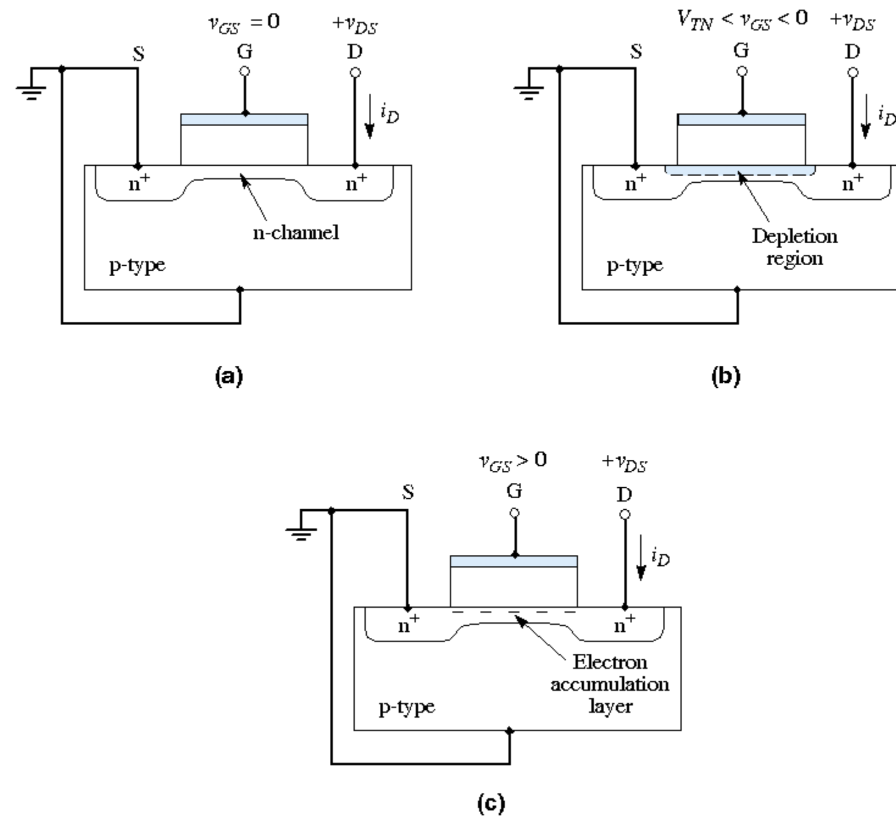


Figure 5.12 Cross section of an n-channel depletion mode MOSFET for: (a) $v_{GS} = 0$, (b) $v_{GS} < 0$, and (c) $v_{GS} > 0$

I-V Curves and Circuit Symbols for Depletion-mode MOSFET

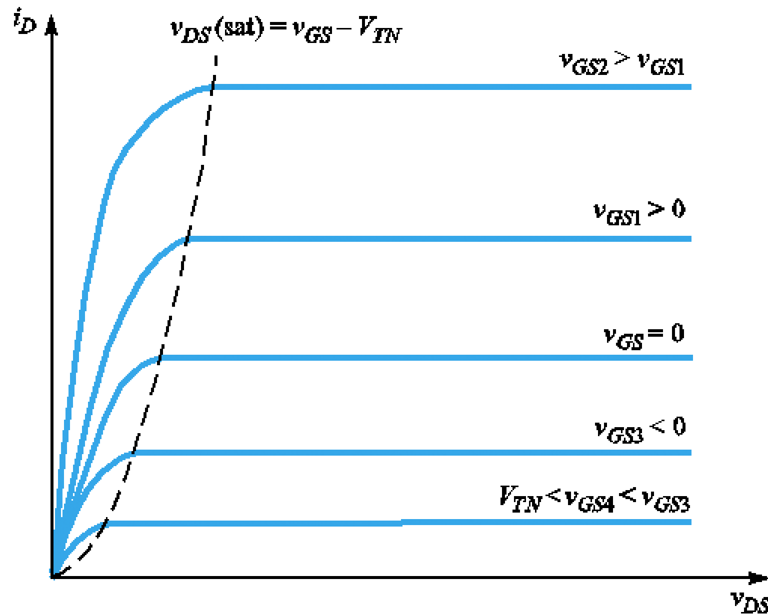
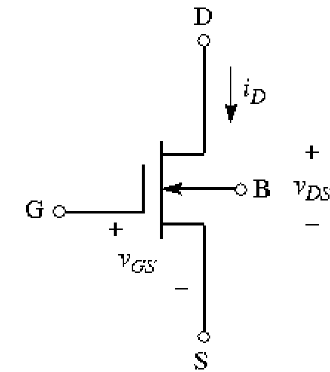


Figure 5.13 Family of i_D vesus v_{DS} curves for an n-channel depletion mode MOSFET



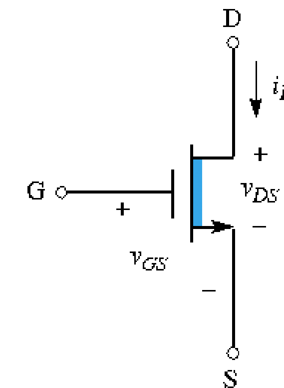
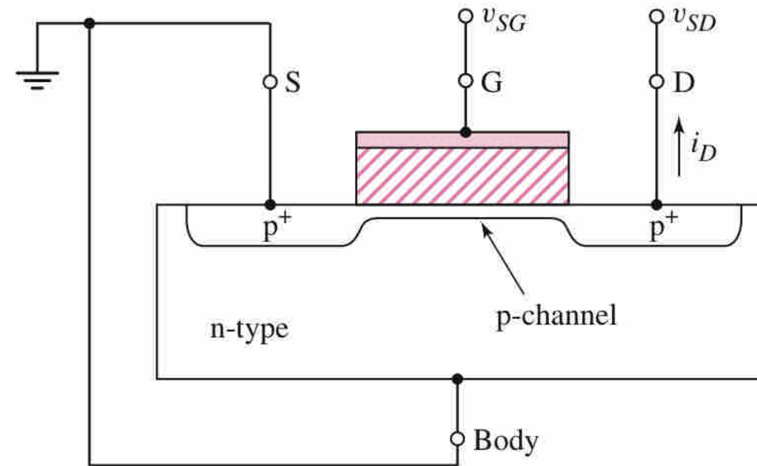
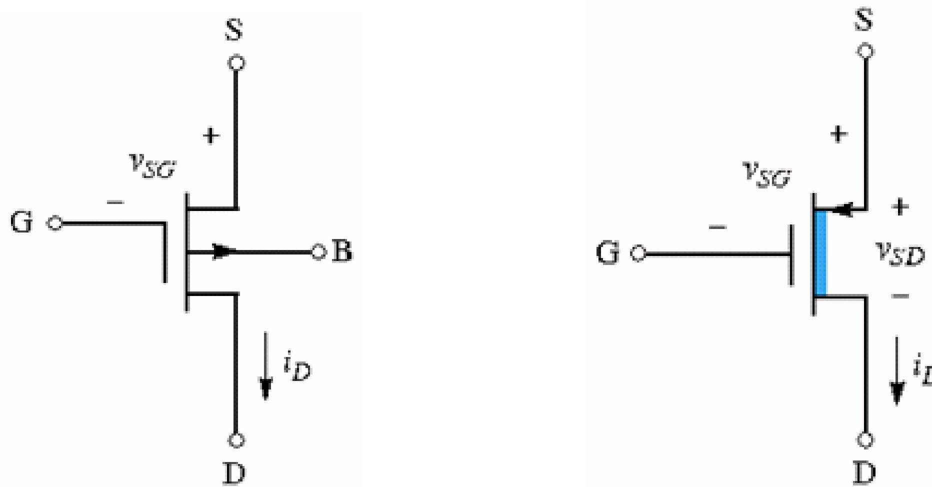


Figure 5.14 The n-channel depletion-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

Depletion-Mode PMOS Circuit Symbols



- Depletion-Mode PMOS Circuit Symbols



CMOS

- Complement MOS (CMOS) technology uses both NMOS and PMOS in the same circuit.
- To design electrically equivalent NMOS and PMOS devices, adjusting the W/L ratios of the transistors is required.

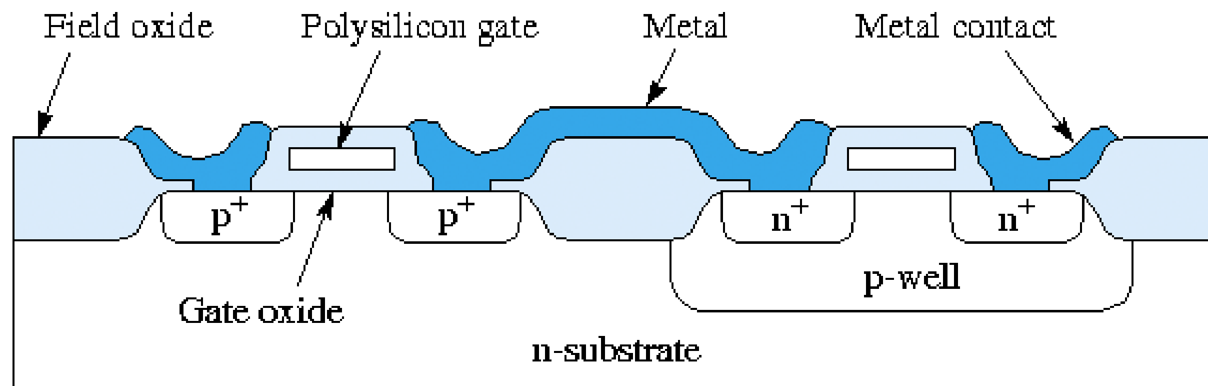


Figure 5.18 Cross sections of n-channel and p-channel transistors fabricated with a p-well CMOS technology

Summary of MOS Transistor Operation

Table 5.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

Finite Output Resistance

- For $v_{DS} > v_{DS(\text{sat})}$, the actual point in the channel at which the inversion charge goes to zero moves away from the drain terminal. The effective channel length decreases, producing the phenomenon called channel length modulation.
- Actual I-V Curves

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})]$$

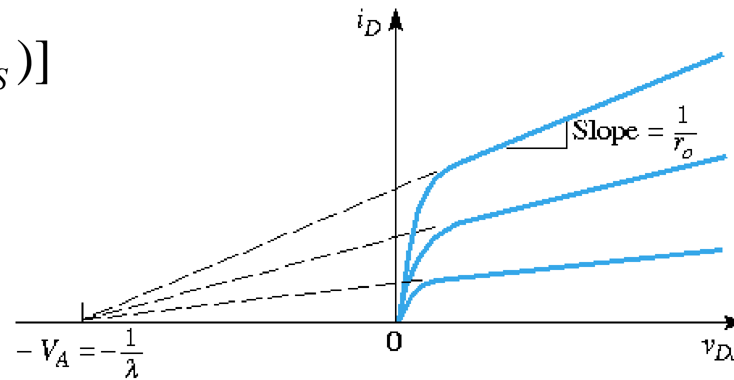


Figure 5.19 Effect of channel length modulation, resulting in a finite output resistance

- The Output Resistance

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}} = [\lambda K_n(V_{GSQ} - V_{TN})^2]^{-1}$$

$$r_o \approx [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

Body Effect

- The threshold voltage is constant only when the substrate (body) is connected to the source.
- The threshold voltage changes due to the biased voltage offset between the source and the substrate. This is called the body effect.

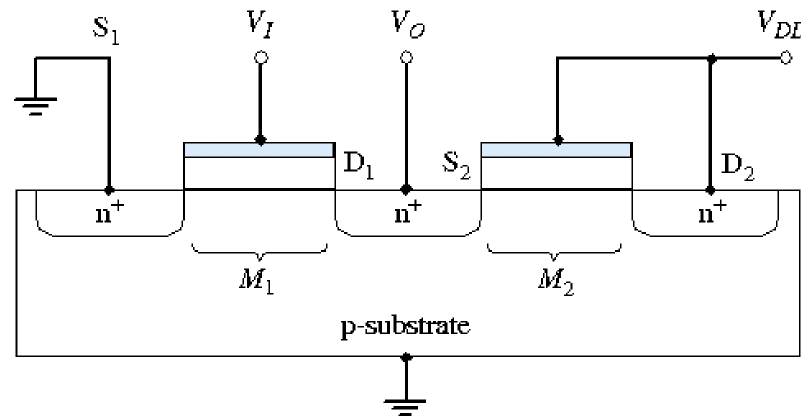


Figure 5.20 Two n-channel MOSFETs fabricated in series in the same substrate

$$V_{TN} = V_{TN0} + \gamma[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}]$$

V_{TN0} : threshold voltage for $v_{SB} = 0$

γ : body-effect parameter, typically 0.5

ϕ_f : semiconductor parameter, typically 0.35

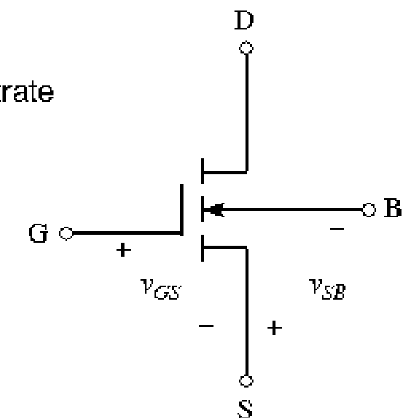


Figure 5.21 An n-channel enhancement-mode MOSFET with a substrate voltage

Subthreshold Conduction

- When v_{GS} is slightly less than V_{TN} , the drain current is not zero. The current is called the subthreshold current.
- The effect may be significant if hundreds or thousands of devices on an integrated circuit are biased just slightly below the threshold voltage, the power supply current will not be zero but may contribute to significant power dissipation in the integrated circuit.

$$i_D = K_n(v_{GS} - V_{TN})^2$$

$$\sqrt{i_D} = \sqrt{K_n}(v_{GS} - V_{TN})$$

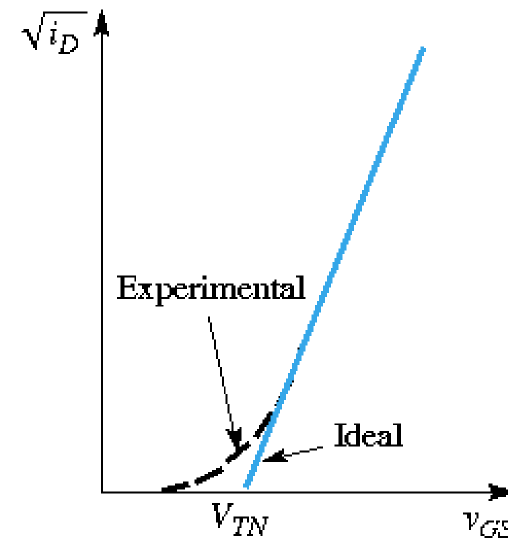


Figure 5.22 Plot of $\sqrt{i_D}$ versus v_{GS} characteristic showing subthreshold conduction

Breakdown and Temperature Effects

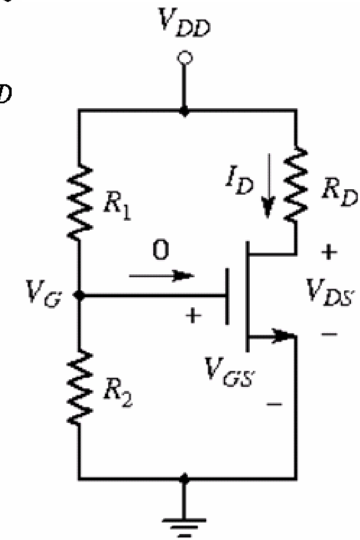
- **Breakdown**: The drain-to-substrate pn junction may break down if the applied drain voltage is too high and avalanche multiplication occurs. The breakdown is the same reverse-biased pn junction breakdown.
- **Punch-through**: when the drain voltage is large enough for the depletion region around the drain to extend completely through the channel to the source terminal. This effect causes the drain current to increase rapidly with only a small increase in drain voltage.
- **Near-avalanche**: The source-substrate-drain structure is equivalent to that of a bipolar transistor. As the device size shrinks, we may begin to see a parasitic bipolar transistor action with increases in the drain voltage. This parasitic action enhances the breakdown effect.
- If the electric field in the oxide becomes large enough, breakdown can also occur in the oxide, which can lead to catastrophic failure.

- **Temperature Effect**
  - ✓ Threshold voltage decreases with temperature, thus the drain current increases with temperature with a given V_{GS}.
  - ✓ The conduction parameter decreases as the temperature increases.
  - ✓ The net effect of increasing temperature is a decrease in drain current at a given V_{GS}.

NMOS Common-Source Circuit

Example 5.3 **Objective:** Calculate the drain current and drain-to-source voltage of a common-source circuit with an n-channel enhancement-mode MOSFET.

For the circuit shown in Figure 5.24(a), assume that $R_1 = 30\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_D = 20\,\text{k}\Omega$, $V_{DD} = 5\,\text{V}$, $V_{TN} = 1\,\text{V}$, and $K_n = 0.1\,\text{mA/V}^2$.



Solution: From the circuit shown in Figure 5.24(b) and Equation (5.12), we have

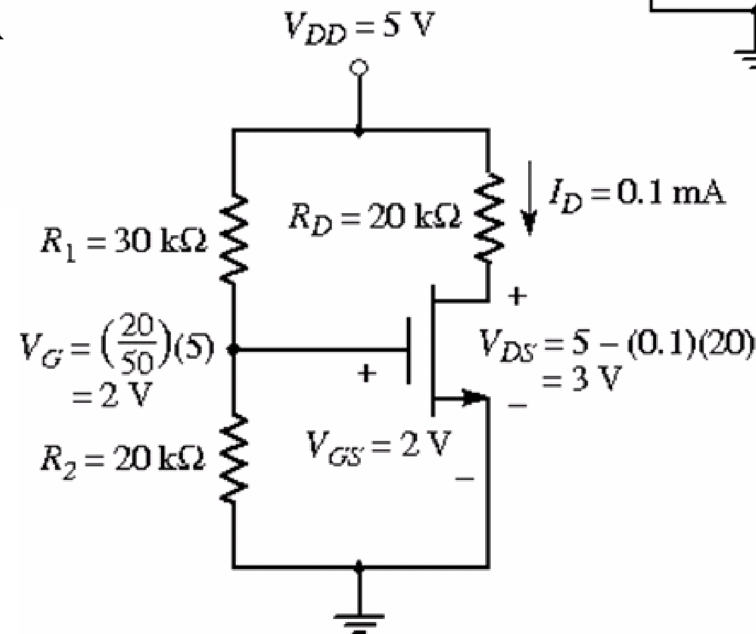
$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{20}{20 + 30}\right)(5) = 2\,\text{V}$$

Assuming the transistor is biased in the saturation region, the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = (0.1)(2 - 1)^2 = 0.1\,\text{mA}$$

and the drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D = 5 - (0.1)(20) = 3\,\text{V}$$



PMOS Common-Source Circuit

Example 5.4 **Objective:** Calculate the drain current and source-to-drain voltage of a common-source circuit with a p-channel enhancement-mode MOSFET.

Consider the circuit shown in Figure 5.25(a). Assume that $R_1 = R_2 = 50\,\text{k}\Omega$, $V_{DD} = 5\,\text{V}$, $R_D = 7.5\,\text{k}\Omega$, $V_{TP} = -0.8\,\text{V}$, and $K_p = 0.2\,\text{mA/V}^2$.

Solution: From the circuit shown in Figure 5.25(b) and Equation (5.15(a)), we have

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{50}{50+50}\right)(5) = 2.5\,\text{V}$$

The source-to-gate voltage is therefore

$$V_{SG} = V_{DD} - V_G = 5 - 2.5 = 2.5\,\text{V}$$

Assuming the transistor is biased in the saturation region, the drain current is

$$I_D = K_p(V_{SG} + V_{TP})^2 = (0.2)(2.5 - 0.8)^2 = 0.578\,\text{mA}$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D = 5 - (0.578)(7.5) = 0.665\,\text{V}$$

Since $V_{SD} = 0.665\,\text{V}$ is not greater than $V_{SD}(\text{sat}) = V_{SG} + V_{TP} = 2.5 - 0.8 = 1.7\,\text{V}$, the p-channel MOSFET is not biased in the saturation region, as we initially assumed.

In the nonsaturation region, the drain current is given by

$$I_D = K_p[2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2]$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D$$

Combining these two equations, we obtain

$$I_D = K_p[2(V_{SG} + V_{TP})(V_{DD} - I_D R_D) - (V_{DD} - I_D R_D)^2]$$

or

$$I_D = (0.2)[2(2.5 - 0.8)(5 - I_D(7.5)) - (5 - I_D(7.5))^2]$$

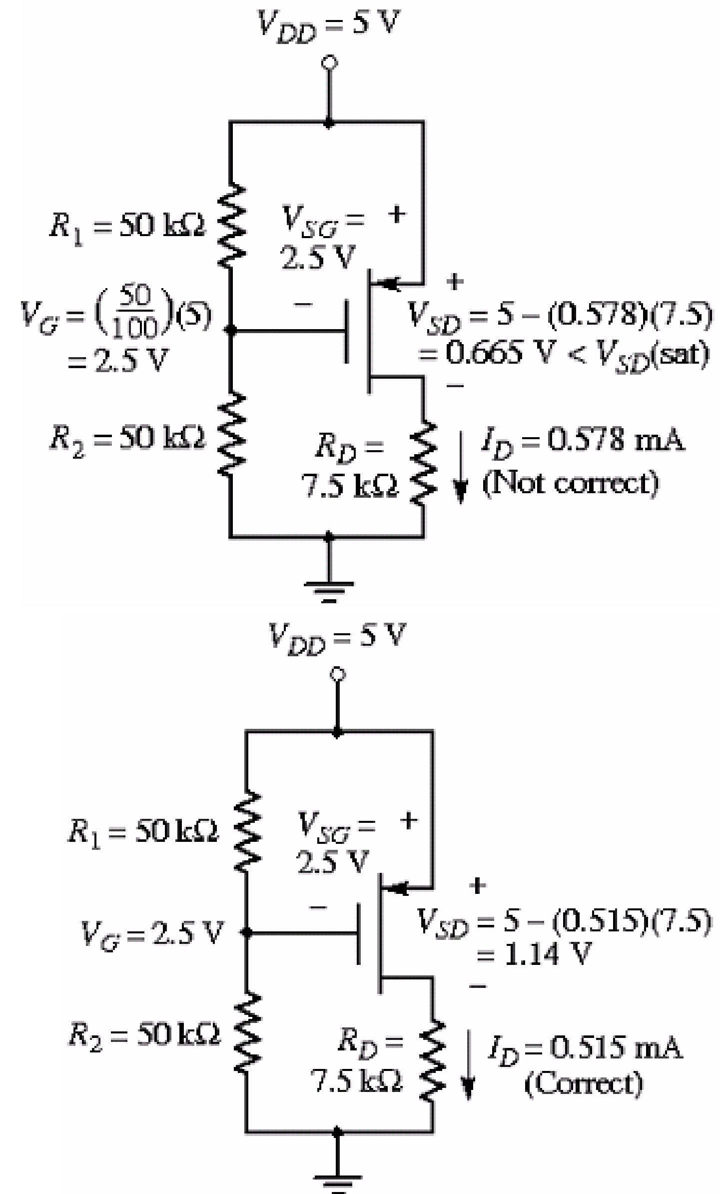
Solving this quadratic equation for I_D, we find

$$I_D = 0.515\,\text{mA}$$

We also find that

$$V_{SD} = 1.14\,\text{V}$$

Therefore, $V_{SD} < V_{SD}(\text{sat})$, which verifies that the transistor is biased in the nonsaturation region.



DESIGN EXAMPLE 3.5

Objective: Design a MOSFET circuit biased with both positive and negative vo ages to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 3.2 Design the circuit such that $I_{DQ} = 0.5$ mA and $V_{DSQ} = 4$ V.

Choices: Standard resistors are to be used in the final design. A transistor with no inal parameters of $k_n' = 80\ \mu A/V^2$, $(W/L) = 6.25$, and $V_{TN} = 1.2$ V is availabl The parameters k_n' and V_{TN} may vary by ± 5 percent.

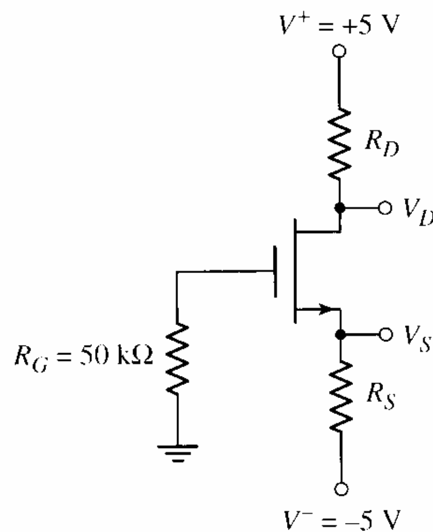


Figure 3.27 Circuit configuration for Example 3.5

Solution: Assuming the transistor is biased in the saturation region, we ha $I_{DQ} = K_n(V_{GS} - V_{TN})^2$. The conduction parameter is

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L} = \frac{0.080}{2} \cdot 6.25 = 0.25\ \text{mA/V}^2$$

Solving for the gate-to-source voltage, we find the required gate-to-source voltage induce the specified drain current.

$$V_{GS} = \sqrt{\frac{I_{DQ}}{K_n}} + V_{TN} = \sqrt{\frac{0.5}{0.25}} + 1.2$$

or

$$V_{GS} = 2.614\ \text{V}$$

Since the gate current is zero, the gate is at ground potential. The voltage at the source terminal is then $V_S = -V_{GS} = -2.614\,\text{V}$. The value of the source resistor is found from

$$R_S = \frac{V_S - V^-}{I_{DQ}} = \frac{-2.614 - (-5)}{0.5}$$

or

$$R_S = 4.77\ \text{k}\Omega$$

The voltage at the drain terminal is determined to be

$$V_D = V_S + V_{DS} = -2.614 + 4 = 1.386\,\text{V}$$

The value of the drain resistor is

$$R_D = \frac{V^+ - V_D}{I_{DQ}} = \frac{5 - 1.386}{0.5}$$

or

$$R_D = 7.23\ \text{k}\Omega$$

We may note that

$$V_{DS} = 4\,V > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 2.61 - 1.2 = 1.41\,\text{V}$$

which means that the transistor is indeed biased in the saturation region.

DESIGN EXAMPLE 3.6

Objective: Design a circuit with a p-channel MOSFET that is biased with both positive and negative voltage supplies to meet a set of specifications.

Specifications: The circuit to be designed is shown in Figure 3.30. Design the circuit such that $I_{DQ} = 100\,\mu\text{A}$, $V_{SDQ} = 3\text{ V}$, and $V_{RS} = 0.8\text{ V}$. The value of the larger bias resistor, either R_1 or R_2, is to be $200\text{ k}\Omega$.

Choices: A transistor with parameters of $K_p = 100\,\mu\text{A/V}^2$ and $V_{TP} = -0.4\text{ V}$ is available. Standard resistor values are to be used in the final design.

Solution: Assuming that the transistor is biased in the saturation region, we have $I_{DQ} = K_p(V_{SG} + V_{TP})^2$. Solving for the source-to-gate voltage, we find the required value of source-to-gate voltage to be

$$V_{SG} = \sqrt{\frac{I_{DQ}}{K_p}} - V_{TP} = \sqrt{\frac{100}{100}} - (-0.4)$$

or

$$V_{SG} = 1.4\text{ V}$$

The voltage at the gate with respect to ground potential is found to be

$$V_G = V^+ - V_{RS} - V_{SG} = 2.5 - 0.8 - 1.4 = 0.3\text{ V}$$

With $V_G > 0$, the resistor R_2 will be the larger of the two bias resistors, so set $R_2 = 200\text{ k}\Omega$. The current through R_2 is then

$$I_{\text{Bias}} = \frac{V_G - V^-}{R_2} = \frac{0.3 - (-2.5)}{200} = 0.014\text{ mA}$$

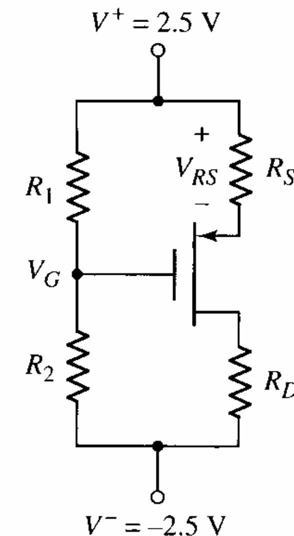


Figure 3.30 Circuit configuration for Example 3.6

Since the current through R_1 is the same, we can find the value of R_1 to be

$$R_1 = \frac{V^+ - V_G}{I_{\text{Bias}}} = \frac{2.5 - 0.3}{0.014}$$

which yields

$$R_1 = 157\,\text{k}\Omega$$

The source resistor value is found from

$$R_S = \frac{V_{RS}}{I_{DQ}} = \frac{0.8}{0.1}$$

or

$$R_S = 8\,\text{k}\Omega$$

The voltage at the drain terminal is

$$V_D = V^+ - V_{RS} - V_{SD} = 2.5 - 0.8 - 3 = -1.3\,\text{V}$$

Then the drain resistor value is found as

$$R_D = \frac{V_D - V^-}{I_{DQ}} = \frac{-1.3 - (-2.5)}{0.1}$$

or

$$R_D = 12\,\text{k}\Omega$$

Trade-offs: Using standard resistors, we find values of $R_D = 12\,\text{k}\Omega$ (designed value), $R_S = 8.2\,\text{k}\Omega$ (from $8\,\text{k}\Omega$), $R_1 = 160\,\text{k}\Omega$ (from $157\,\text{k}\Omega$), and $R_2 = 200\,\text{k}\Omega$

(designed value). Using these standard resistors, we find

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(5) - 2.5 = \left(\frac{200}{200 + 160}\right)(5) - 2.5$$

or

$$V_G = 0.278 \text{ V}$$

We can then write

$$2.5 = I_D R_S + V_{SG} + 0.278$$

where

$$I_D = K_p(V_{SG} + V_{TP})^2$$

We find $V_{SG} = 1.40$ V, $I_{DQ} = 0.10$ mA, and $V_{SDQ} = 2.98$ V. The ideal desi load line and load line using the standard resistor values, along with the Q- values, are shown in Figure 3.31.

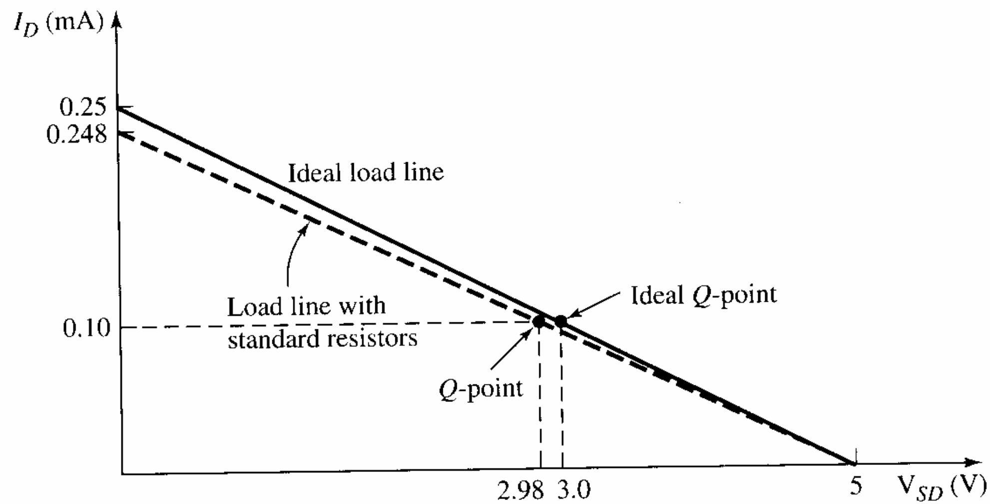


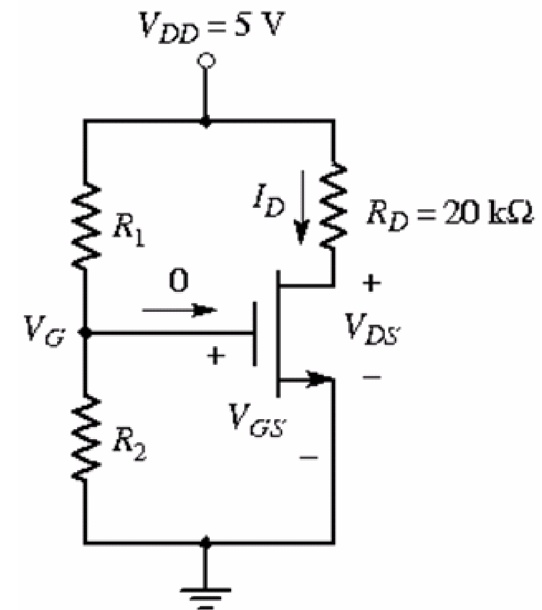
Figure 3.31 Load lines and Q-point values for circuit in Example 3.6.

Load Line

- Load Line

$$V_{DS} = V_{DD} - I_D R_D = 5 - I_D(20)$$

$$I_D = \frac{5}{20} - \frac{V_{DS}}{20} \text{(mA)}$$



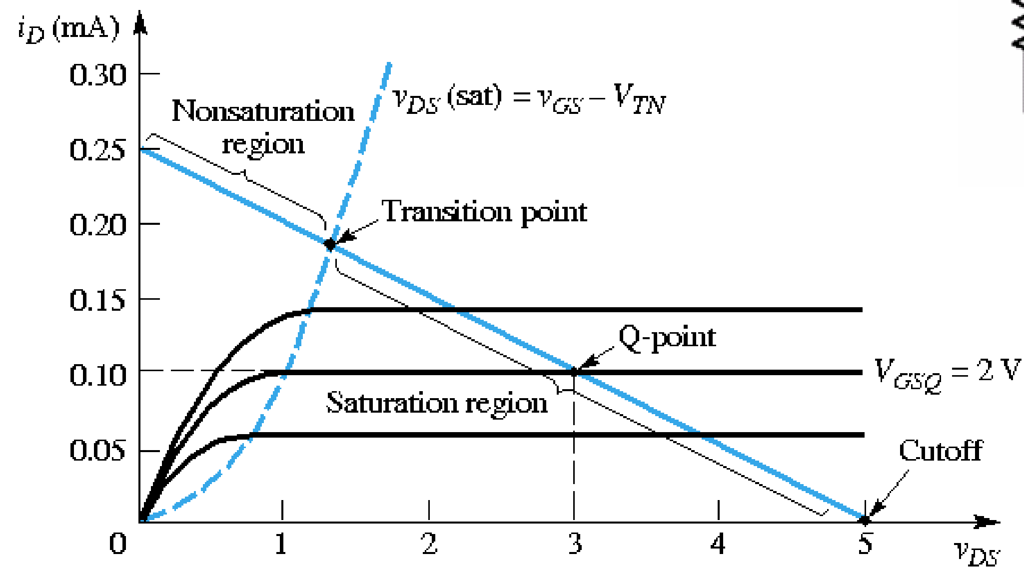


Figure 5.28 Transistor characteristics, v_{DS}(sat) curve, load line, and Q-point for the NMOS common-source circuit in Figure 5.24(b)

Example 5.5 **Objective:** Determine the transition point parameters for a common-source circuit.

Consider the circuit shown in Figure 5.24(b). Assume transistor parameters of $V_{TN} = 1\,\text{V}$ and $K_n = 0.1\,\text{mA/V}^2$.

Solution: At the transition point,

$$V_{DS} = V_{DS}(\text{sat}) = V_{GS} - V_{TN} = V_{DD} - I_D R_D$$

The drain current is still

$$I_D = K_n(V_{GS} - V_{TN})^2$$

Combining the last two equations, we obtain

$$V_{GS} - V_{TN} = V_{DD} - K_n R_D (V_{GS} - V_{TN})^2$$

Rearranging this equation produces

$$K_n R_D (V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - V_{DD} = 0$$

or

$$(0.1)(20)(V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - 5 = 0$$

Solving the quadratic equation, we find that

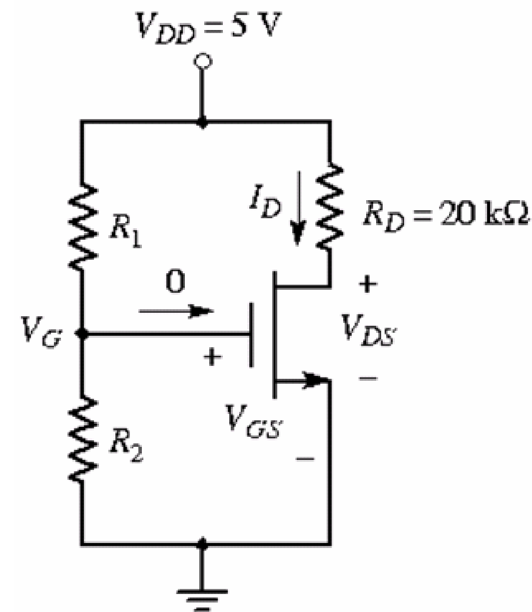
$$V_{GS} - V_{TN} = 1.35\,\text{V} = V_{DS}$$

Therefore,

$$V_{GS} = 2.35\,\text{V}$$

and

$$I_D = (0.1)(2.35 - 1)^2 = 0.182\,\text{mA}$$



DESIGN EXAMPLE 3.8

Objective: Design the dc bias of a MOSFET circuit to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 3.34. The quiescent Q-point values are to be $I_{DQ} = 0.25$ mA and $V_{DSQ} = 4$ V. The voltage across R_S should be $V_{RS} \cong 1$ V. The current in the bias resistors should be approximately 20 μA.

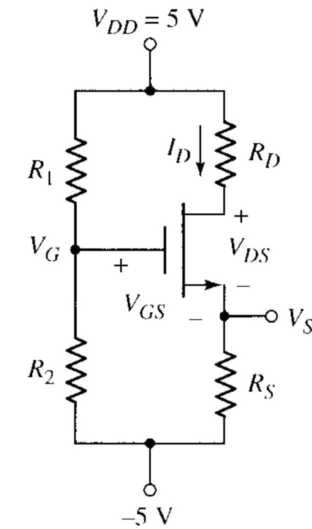


Figure 3.34 NMOS common-source circuit with source resistor

Choices: Discrete resistors are to be used in the final design. A transistor with parameters of $k_n' = 80\ \mu A/V^2$, $W/L = 4$, and $V_{TN} = 1.2$ V is available. The resistors R_D and R_S have tolerances of ± 10 percent.

Solution: The source resistor is determined as

$$R_S = \frac{V_{RS}}{I_{DQ}} = \frac{1}{0.25} = 4\ k\Omega$$

The drain resistor is found from a KVL equation around the drain-source loop. We have

$$5 = I_{DQ}R_D + V_{DS} + I_{DQ}R_S - 5$$

or

$$5 = (0.25)R_D + 4 + (0.25)(4) - 5$$

which yields

$$R_D = 20\ k\Omega$$

Since the current through the bias resistors is to be 20 μA, we can find

$$R_1 + R_2 = \frac{5 + 5}{0.020} = 500\ k\Omega$$

The gate-to-source voltage can be found from

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} (V_{GS} - V_{TN})^2$$

or

$$0.25 = \frac{0.080}{2} \cdot 4(V_{GS} - 1.2)^2$$

which yields

$$V_{GS} = 2.45\ \text{V}$$

We can write

$$V_{GS} = V_G - V_S = \left[\left(\frac{R_2}{R_1 + R_2}\right)(10) - 5\right] - [I_D R_S - 5]$$

or

$$2.45 = \left[\left(\frac{R_2}{500}\right)(10) - 5\right] - [(0.25)(4) - 5]$$

which yields

$$R_2 = 172.5\ \text{k}\Omega$$

Then

$$R_1 = 327.5\ \text{k}\Omega$$

Design Example 5.7 **Objective:** Design a MOSFET circuit biased with a constant-current source.

The parameters of the transistor in the circuit shown in Figure 5.30(a) are $V_{TN} = 0.8$ V, $k_n' = 80\ \mu A/V^2$, and $W/L = 3$. Design the circuit such that the quiescent values are $I_D = 250\ \mu A$ and $V_D = 2.5$ V.

Solution: The dc equivalent circuit is shown in Figure 5.30(b). Since $v_i = 0$, the gate is at ground potential and there is no gate current through R_G.

Assuming the transistor is biased in the saturation region, we have

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L}(V_{GS} - V_{TN})^2$$

or

$$250 = \left(\frac{80}{2}\right) \cdot (3)(V_{GS} - 0.8)^2$$

which yields

$$V_{GS} = 2.24\ \text{V}$$

The voltage at the source terminal is $V_S = -V_{GS} = -2.24$ V.

The drain current can also be written as

$$I_D = \frac{5 - V_D}{R_D}$$

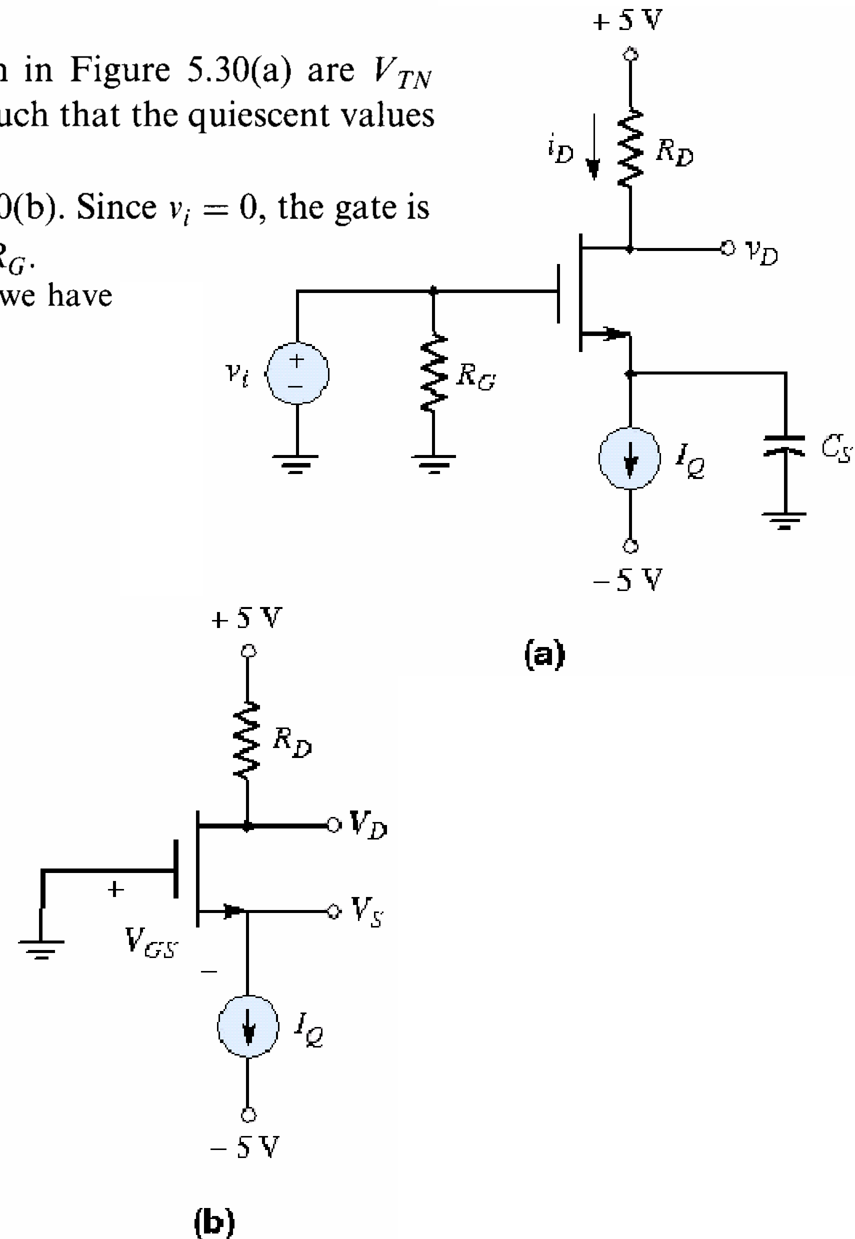
For $V_D = 2.5$ V, we have

$$R_D = \frac{5 - 2.5}{0.25} = 10\ \text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = V_D - V_S = 2.5 - (-2.24) = 4.74\ \text{V}$$

Since $V_{DS} = 4.74\ \text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 2.24 - 0.8 = 1.44$ V, the transistor is biased in the saturation region, as initially assumed.



Nonlinear Resistor

- An enhancement-mode MOSFET is used as a nonlinear resistor.
- The transistor is always biased in the saturation region and called a load device.

$$v_{DS} = v_{GS} > v_{DS(Sat)} = v_{GS} - V_{TN}, \quad V_{TN} > 0$$

$$i_D = K_n (v_{GS} - V_{TN})^2 = K_n (v_{DS} - V_{TN})^2$$

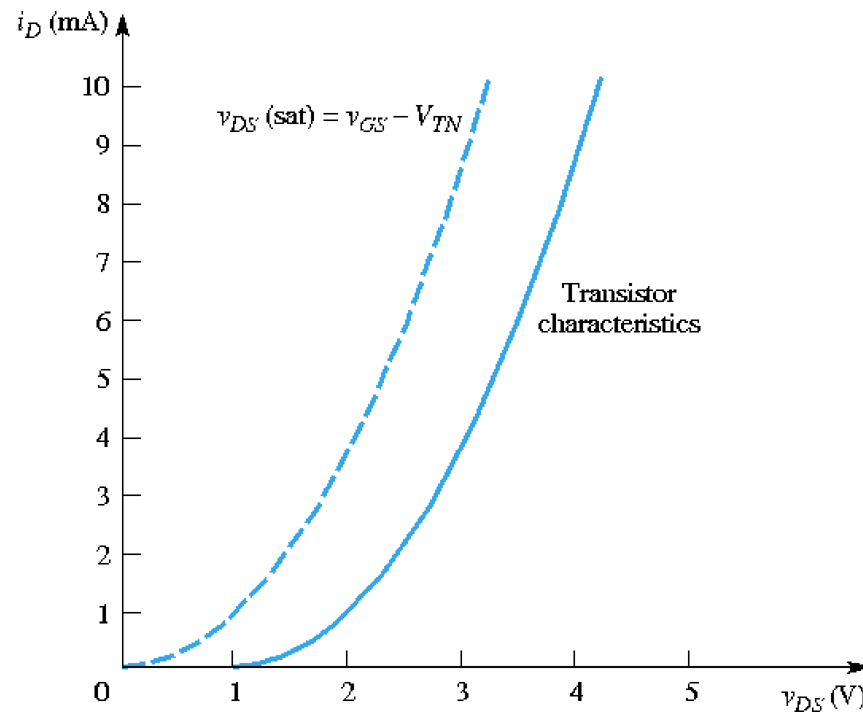


Figure 5.33 Current–voltage characteristic of an enhancement load device

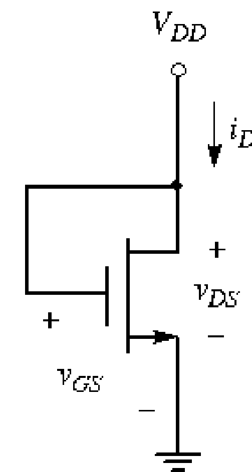


Figure 5.32 Enhancement-mode NMOS device with the gate connected to the drain

Example 5.8 **Objective:** Calculate the characteristics of a circuit containing an enhancement load device.

Consider the circuit shown in Figure 5.34 with transistor parameters $V_{TN} = 0.8\,\text{V}$ and $K_n = 0.05\,\text{mA/V}^2$.

Solution: Since the transistor is biased in the saturation region, the dc drain current is given by

$$I_D = K_n(V_{GS} - V_{TN})^2$$

and the dc drain-to-source voltage is

$$V_{DS} = V_{GS} = 5 - I_D R_S$$

Combining these two equations, we obtain

$$V_{GS} = 5 - K_n R_S (V_{GS} - V_{TN})^2$$

Substituting parameter values, we obtain

$$V_{GS} = 5 - (0.05)(10)(V_{GS} - 0.8)^2$$

which can be written as

$$0.5V_{GS}^2 + 0.2V_{GS} - 4.68 = 0$$

The two possible solutions are

$$V_{GS} = -3.27\,\text{V} \quad \text{and} \quad V_{GS} = +2.87\,\text{V}$$

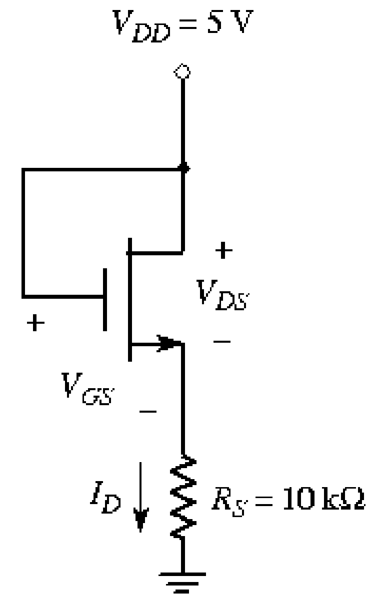


Figure 5.34 Circuit containing an enhancement load device

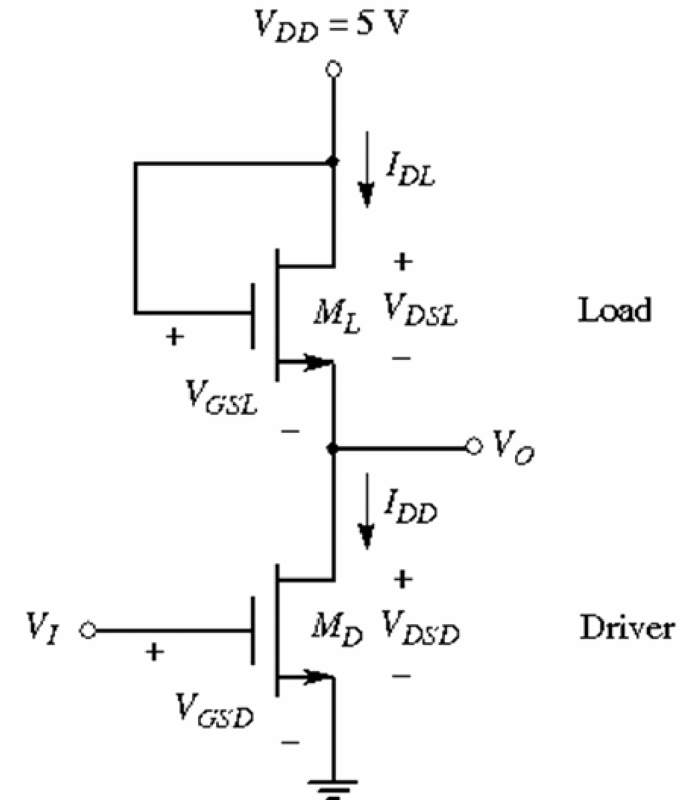
Since we are assuming the transistor is conducting, the gate-to-source voltage must be greater than the threshold voltage. We therefore have the following solution:

$$V_{GS} = V_{DS} = 2.87\,\text{V} \quad \text{and} \quad I_D = 0.213\,\text{mA}$$

Example 5.9 **Objective:** Determine the dc transistor currents and voltages in a circuit containing an enhancement load device.

The transistors in the circuit shown in Figure 5.35 have parameters $V_{TND} = V_{TNL} = 1\,\text{V}$, $K_{nD} = 50\,\mu\text{A/V}^2$, and $K_{nL} = 10\,\mu\text{A/V}^2$. (The subscript D applies to the driver transistor and the subscript L applies to the load transistor.) Determine V_O for $V_I = 5\,\text{V}$ and $V_I = 1.5\,\text{V}$.

Solution: ($V_I = 5\,\text{V}$) Assume that the driver transistor M_D is biased in the nonsaturation region. The drain current in the load device is equal to the drain current in the driver transistor. Writing these currents in generic form, we have



$$I_{DD} = I_{DL}$$

or

$$K_{nD}[2(V_{GSD} - V_{TND})V_{DSD} - V_{DSD}^2] = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Since $V_{GSD} = V_I$, $V_{DSD} = V_O$, and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, then

$$K_{nD}[2(V_I - V_{TND})V_O - V_O^2] = K_{nL}[V_{DD} - V_O - V_{TNL}]^2$$

Substituting numbers, we find

$$(50)[2(5-1)V_O - V_O^2] = (10)[5 - V_O - 1]^2$$

Rearranging the terms provides

$$3V_O^2 - 24V_O + 8 = 0$$

Using the quadratic formula, we obtain two possible solutions:

$$V_O = 7.65\,\text{V} \quad \text{or} \quad V_O = 0.349\,\text{V}$$

Since the output voltage cannot be greater than the supply voltage $V_{DD} = 5\,\text{V}$, the valid solution is $V_O = 0.349\,\text{V}$.

Also, since $V_{DSD} = V_O = 0.349\,\text{V} < V_{GSD} - V_{TND} = 5 - 1 = 4\,\text{V}$, the driver M_D is biased in the nonsaturation region, as initially assumed.

The current can be determined from

$$I_D = K_{nL}(V_{GSL} - V_{TNL})^2 = K_{nL}(V_{DD} - V_O - V_{TNL})^2$$

or

$$I_D = (10)(5 - 0.349 - 1)^2 = 133\,\mu\text{A}$$

Solution: ($V_I = 1.5\,\text{V}$) Assume that the driver transistor M_D is biased in the saturation region. Equating the currents in the two transistors and writing the current equations in generic form, we have

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[V_{GSD} - V_{TND}]^2 = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Again, since $V_{GSD} = V_I$ and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, then

$$K_{nD}[V_I - V_{TND}]^2 = K_{nL}[V_{DD} - V_O - V_{TNL}]^2$$

Substituting numbers and taking the square root, we find

$$\sqrt{50}[1.5 - 1] = \sqrt{10}[5 - V_O - 1]$$

which yields $V_O = 2.88\,\text{V}$.

Since $V_{DSD} = V_O = 2.88\,\text{V} > V_{GSD} - V_{TND} = 1.5 - 1 = 0.5\,\text{V}$, the driver transistor M_D is biased in the saturation region, as initially assumed.

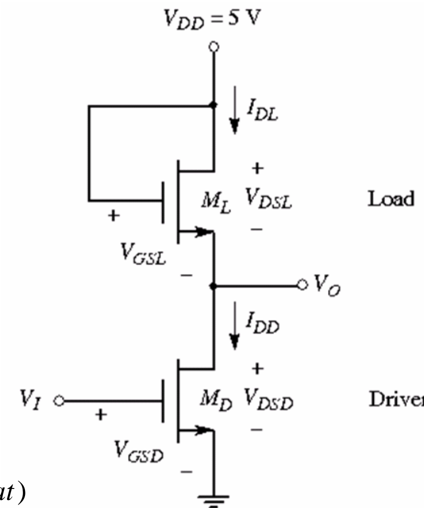
The current is

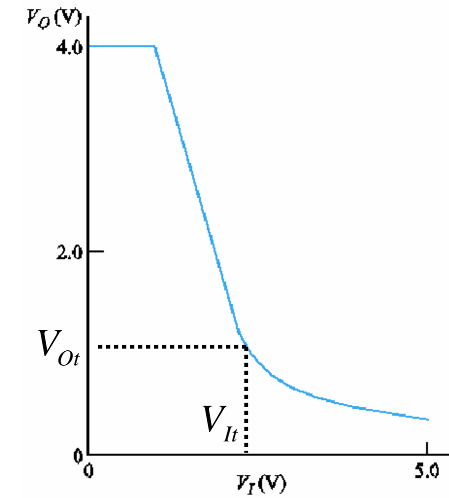
$$I_D = K_{nD}(V_{GSD} - V_{TND})^2 = (50)(1.5 - 1)^2 = 12.5\,\mu\text{A}$$

The Transition Point for Saturation and Non-saturation Regions

(1) Load Device Transistor Characteristics

$$I_{DL} = K_{nL}(V_{GSL} - V_{TNL})^2$$
$$= K_{nL}(V_{DD} - V_{TNL} - V_O)^2$$





(2) Transition Point for the Driver Transistor

$$V_{DSD(Sat)} = V_{GSD} - V_{TND}$$

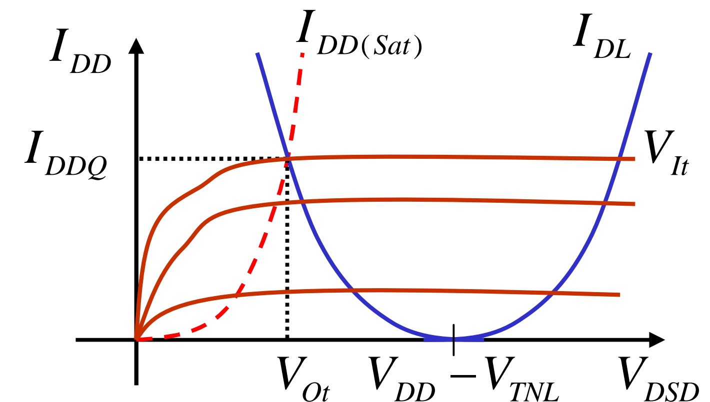
The current in the saturation region,

$$I_{DD(Sat)} = K_{nD}(V_{GSD} - V_{TND})^2 = K_{nD}V_{DSD(Sat)}^2$$

(3) For the transition input voltage $V_{GSD} = V_{It}$

The transition output voltage $V_O = V_{Ot} = V_{DSD(Sat)} = V_{It} - V_{TND}$

$$I_{DD(Sat)} = I_{DL}$$
$$K_{nD}(V_{It} - V_{TND})^2 = K_{nL}(V_{DD} - V_{TNL} - V_{It} + V_{TND})^2$$
$$\sqrt{K_{nD}}(V_{It} - V_{TND}) = \sqrt{K_{nL}}(V_{DD} - V_{TNL} - V_{It} + V_{TND})$$
$$V_{It} = \frac{V_{DD} - V_{TNL} + V_{TND}(1 + \sqrt{K_{nD}/K_{nL}})}{1 + \sqrt{K_{nD}/K_{nL}}}$$



Depletion-mode MOSFET as a Load Device

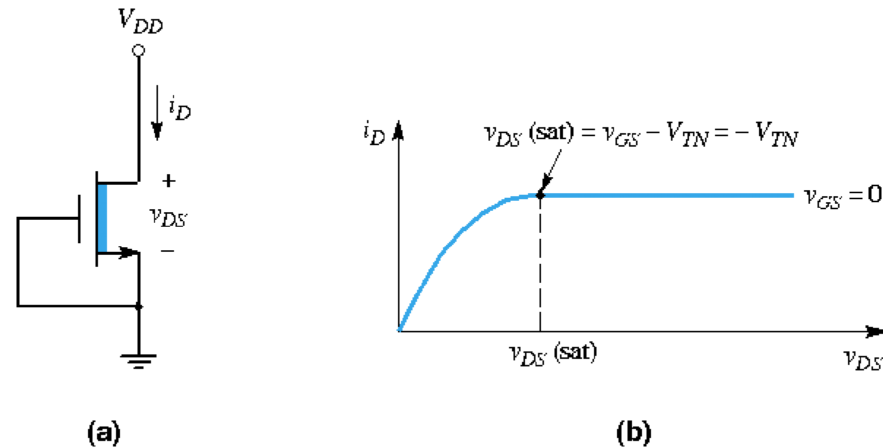


Figure 5.37 (a) Depletion-mode NMOS device with the gate connected to the source and (b) current–voltage characteristics

Example 5.10 **Objective:** Calculate the characteristics of a circuit containing a depletion load device.

For the circuit shown in Figure 5.38 the transistor parameters are $V_{TN} = -2$ V and $K_n = 0.1\,\text{mA/V}^2$. Assume that $V_{DD} = 5$ V and $R_S = 5\,\text{k}\Omega$.

Solution: If we assume that the transistor is biased in the saturation region, then the dc drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = K_n(-V_{TN})^2 = (0.1)(-(-2))^2 = 0.4\,\text{mA}$$

In this case, the transistor is acting as a constant-current source. The dc drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_S = 5 - (0.4)(5) = 3\,\text{V}$$

Since

$$V_{DS} = 3\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 0 - (-2) = 2\,\text{V}$$

the transistor is biased in the saturation region.

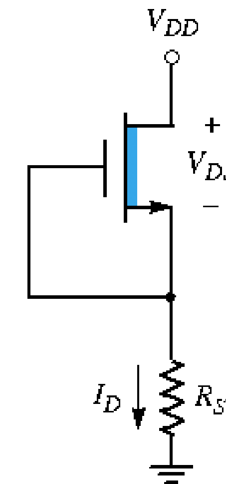


Figure 5.38 Circuit containing a depletion load device

Example 5.11 **Objective:** Determine the dc transistor currents and voltages in a circuit containing a depletion load device.

Consider the circuit shown in Figure 5.39 with transistor parameters: $V_{TND} = 1\,\text{V}$, $V_{TNL} = -2\,\text{V}$, $K_{nD} = 50\,\mu\text{A/V}^2$, and $K_{nL} = 10\,\mu\text{A/V}^2$. Determine V_O for $V_I = 5\,\text{V}$.

Solution: Assume the driver transistor M_D is biased in the nonsaturation region and the load transistor M_L is biased in the saturation region. The drain currents in the two transistors are equal. In generic form, these currents are

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[2(V_{GSD} - V_{TND})V_{DSD} - V_{DSD}^2] = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Since $V_{GSD} = V_I$, $V_{DSD} = V_O$, and $V_{GSL} = 0$, then

$$K_{nD}[2(V_I - V_{TND})V_O - V_O^2] = K_{nL}[-V_{TNL}]^2$$

Substituting numbers, we find

$$(50)[2(5-1)V_O - V_O^2] = (10)[-(-2)]^2$$

Rearranging the terms produces

$$5V_O^2 - 40V + 4 = 0$$

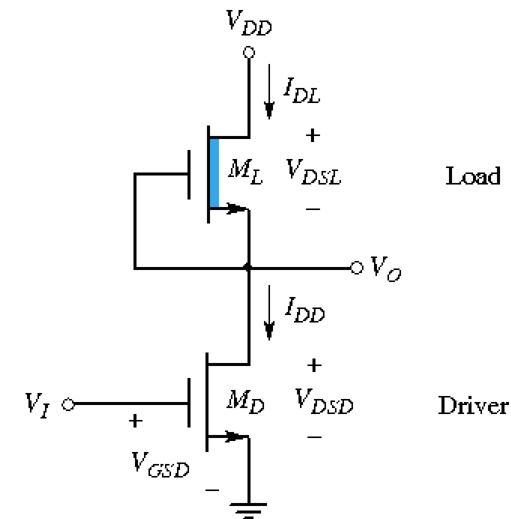


Figure 5.39 Circuit with depletion load device and NMOS driver

Using the quadratic formula, we obtain two possible solutions:

$$V_O = 7.90\,\text{V} \quad \text{or} \quad V_O = 0.10\,\text{V}$$

Since the output voltage cannot be greater than the supply voltage $V_{DD} = 5\,\text{V}$, the valid solution is $V_O = 0.10\,\text{V}$.

The current is

$$I_D = K_{nL}(-V_{TNL})^2 = (10)[-(-2)]^2 = 40\,\mu\text{A}$$

CMOS Inverter

Example 5.12 **Objective:** Determine the voltage transfer characteristic of the CMOS inverter using a PSpice analysis.

For the circuit shown in Figure 5.41, assume transistor parameters of $V_{TN} = 1\,\text{V}$, $V_{TP} = -1\,\text{V}$, and $K_n = K_p$. Also assume $V_{DD} = 5\,\text{V}$ and $V_G = 3.25\,\text{V}$.

Solution: The voltage transfer characteristics are shown in Figure 5.42. In this case, there is a region, as was the case for an NMOS inverter with depletion load, in which both transistors are biased in the saturation region, and the input voltage is a constant over this transition region for the assumption that the channel length modulation parameter λ is zero.

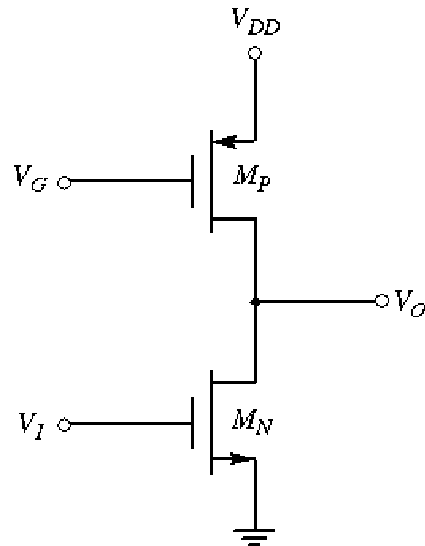


Figure 5.41 Example of CMOS inverter

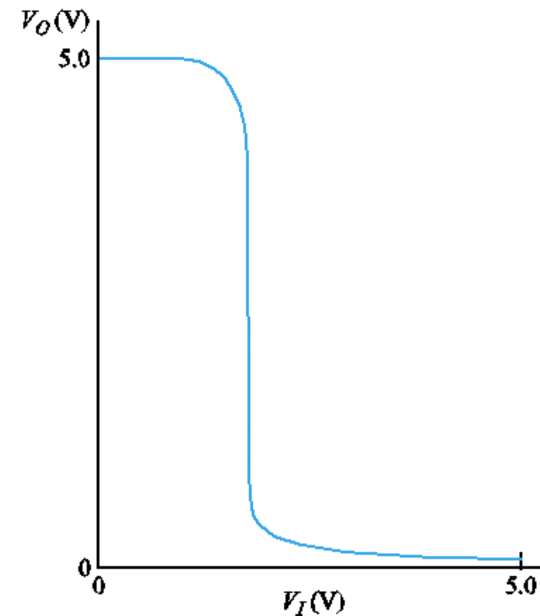


Figure 5.42 Voltage transfer characteristics of CMOS inverter in Figure 5.41

NMOS Inverter

- If $v_I < V_{TN}$, the transistor is in cut-off.

$$i_D = 0$$
$$v_O = V_{DD}$$

- If $v_I > V_{TN}$ (and make $v_I - V_{TN} > v_{DS}$), the transistor is biased in the non-saturation region.

$$i_D = K_n[2(v_I - V_{TN})v_O - v_O^2]$$
$$v_O = v_{DD} - i_D R_D$$

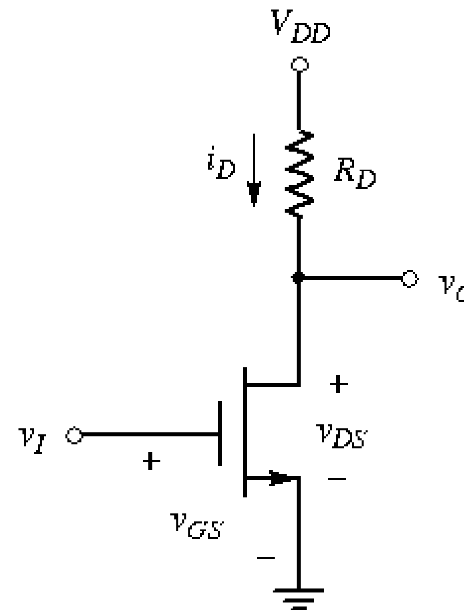


Figure 5.44 NMOS inverter circuit

Design Example 5.14 **Objective:** Design the size of a power MOSFET to meet the specification of a particular switch application.

The load in the inverter circuit in Figure 5.44 is a coil of an electromagnet that requires a current of 0.5 A when turned on. The effective load resistance varies between 8 and 10 Ω, depending on temperature and other variables. A 10 V power supply is available. The transistor parameters are $k_n' = 80\ \mu A/V^2$ and $V_{TN} = 1$ V.

Solution: One solution is to bias the transistor in the saturation region so that the current is constant, independent of the load resistance.

The minimum V_{DS} value is 5 V. We need $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN}$. If we bias the transistor at $V_{GS} = 5$ V, then the transistor will always be biased in the saturation region. We can then write

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L}(V_{GS} - V_{TN})^2$$

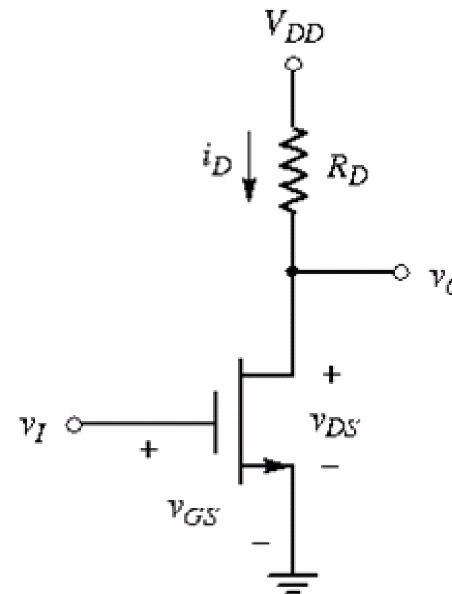
or

$$0.5 = \frac{80 \times 10^{-6}}{2}\left(\frac{W}{L}\right) \cdot (5 - 1)^2$$

which yields $W/L = 781$.

The maximum power dissipated in the transistor is

$$P(\max) = V_{DS}(\max) \cdot I_D = (6) \cdot (0.5) = 3\text{ W}$$



Digital Logic Gate

Example 5.15 **Objective:** Determine the currents and voltages in a digital logic gate, for various input conditions.

Consider the circuit shown in Figure 5.46 with circuit and transistor parameters $R_D = 20\,\text{k}\Omega$, $K_n = 0.1\,\text{mA/V}^2$, and $V_{TN} = 0.8\,\text{V}$.

Solution: For $V_1 = V_2 = 0$, both M_1 and M_2 are cut off and $V_O = V_{DD} = 5\,\text{V}$. For $V_1 = 5\,\text{V}$ and $V_2 = 0$, the transistor M_1 is biased in the nonsaturation region, and we can write

$$I_R = I_{D1} = \frac{5 - V_O}{R_D} = K_n[2(V_1 - V_{TN})V_O - V_O^2]$$

Solving for the output voltage V_O, we obtain $V_O = 0.29\,\text{V}$.

The currents are

$$I_R = I_{D1} = \frac{5 - 0.29}{20} = 0.236\,\text{mA}$$

For $V_1 = 0$ and $V_2 = 5\,\text{V}$, we have $V_O = 0.29\,\text{V}$ and $I_R = I_{D2} = 0.236\,\text{mA}$. When both inputs go high to $V_1 = V_2 = 5\,\text{V}$, we have $I_R = I_{D1} + I_{D2}$, or

$$\frac{5 - V_O}{R_D} = K_n[2(V_1 - V_{TN})V_O - V_O^2] + K_n[2(V_2 - V_{TN})V_O - V_O^2]$$

which can be solved for V_O to yield $V_O = 0.147\,\text{V}$.

The currents are

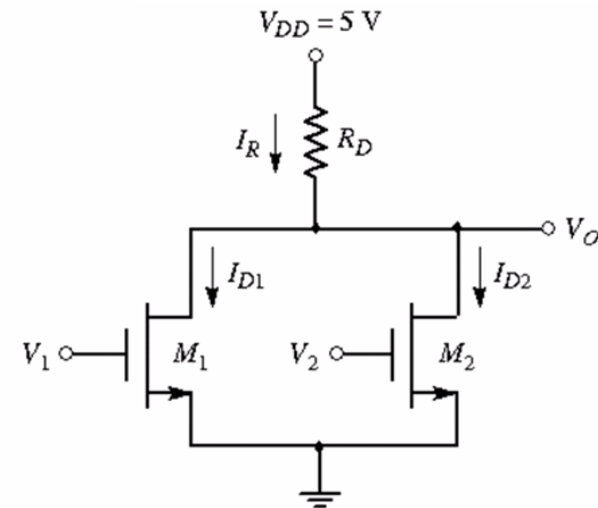
$$I_R = \frac{5 - 0.147}{20} = 0.243\,\text{mA}$$

and

$$I_{D1} = I_{D2} = \frac{I_R}{2} = 0.121\,\text{mA}$$

Table 5.2 NMOS NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	High
5	0	Low
0	5	Low
5	5	Low



MOS Small-Signal Amplifier

- We can establish a particular Q-point on the load line by designing the ratio of the bias resistors R_1 and R_2.

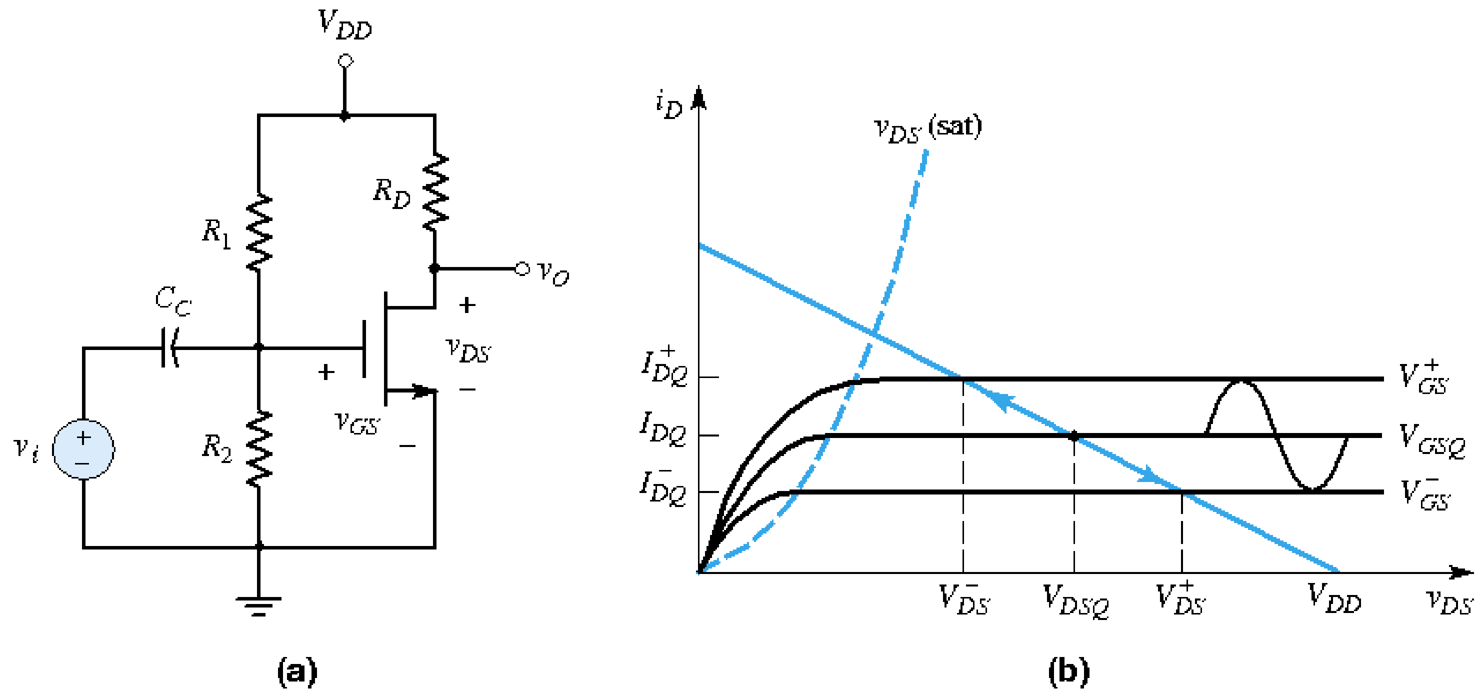


Figure 5.47 (a) An NMOS common-source circuit with a time-varying signal coupled to the gate and (b) transistor characteristics, load line, and superimposed sinusoidal signals

Constant-Current Biasing

EXAMPLE **3.17**

Objective: Analyze the circuit shown in Figure 3.53(a). Determine the bias current I_{Q1}, the gate-to-source voltages of the transistors, and the drain-to-source voltage of M_1.

Assume circuit parameters of $I_{REF1} = 200\ \mu A$, $V^+ = 2.5$ V, and $V^- = -2.5$ V. Assume transistor parameters of $V_{TN} = 0.4$ V (all transistors), $\lambda = 0$ (all transistors), $K_{n1} = 0.25\ mA/V^2$, and $K_{n2} = K_{n3} = 0.15\ mA/V^2$.

Solution: The drain current in M_3 is $I_{D3} = I_{REF1} = 200\ \mu A$ and is given by the relation $I_{D3} = K_{n3}(V_{GS3} - V_{TN})^2$ (the transistor is biased in the saturation region). Solving for the gate-to-source voltage, we find

$$V_{GS3} = \sqrt{\frac{I_{D3}}{K_{n3}}} + V_{TN} = \sqrt{\frac{0.2}{0.15}} + 0.4$$

or

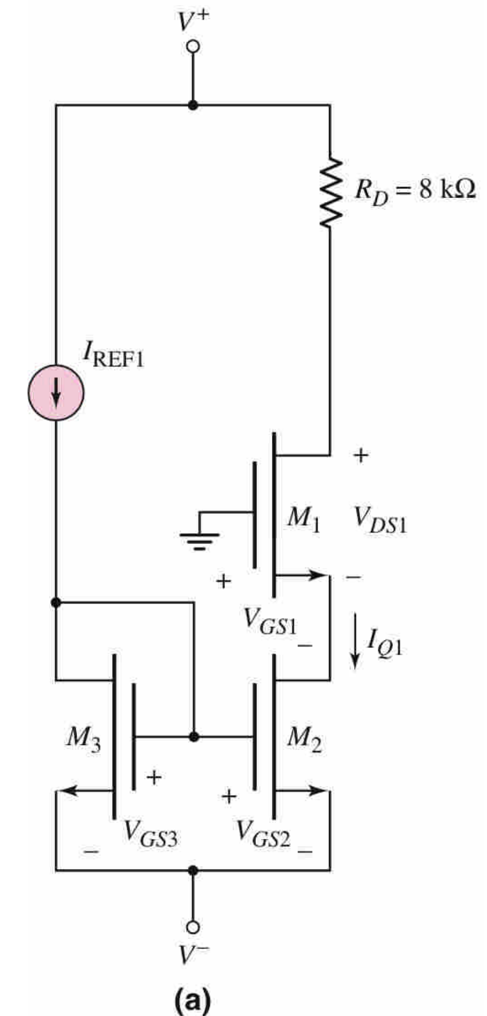
$$V_{GS3} = 1.555 \text{ V}$$

We note that $V_{GS3} = V_{GS2} = 1.555$ V. We can write

$$I_{D2} = I_{Q1} = K_{n2}(V_{GS2} - V_{TN})^2 = 0.15(1.555 - 0.4)^2$$

or

$$I_{Q1} = 200\ \mu A$$



(a)

The gate-to-source voltage V_{GS1} (assuming M_1 is biased in the saturation region) can be written as

$$V_{GS1} = \sqrt{\frac{I_{Q1}}{K_{n1}}} + V_{TN} = \sqrt{\frac{0.2}{0.25}} + 0.4$$

or

$$V_{GS1} = 1.29 \text{ V}$$

The drain-to-source voltage is found from

$$V_{DS1} = V^+ - I_{Q1}R_D - (-V_{GS1})$$
$$= 2.5 - (0.2)(8) - (-1.29)$$

or

$$V_{DS1} = 2.19 \text{ V}$$

We may note that M_1 is indeed biased in the saturation region.

Comment: Since the current mirror transistors M_2 and M_3 are matched (identical parameters) and since the gate-to-source voltages are the same in the two transistors, the bias current, I_{Q1}, is equal to (i.e., mirrors) the reference current, I_{REF1}.

EXAMPLE 3.18

Objective: Design the circuit shown in Figure 3.53(b) to provide a bias current of $I_{Q2} = 150\ \mu A$.

Assume circuit parameters of $I_{REF2} = 250\ \mu A$, $V^+ = 3$ V, and $V^- = -3$ V. Assume transistor parameters of $V_{TP} = -0.6$ V (all transistors), $\lambda = 0$ (all transistors), $k'_p = 40\ \mu A/V^2$ (all transistors), $W/L_C = 15$, and $W/L_A = 25$.

Solution: Since the bias current I_{Q2} and reference current I_{REF2} are not equal, the W/L ratios of the current mirror transistors, M_C and M_B, will not be the same.

For M_C, since the transistor is biased in the saturation region, we have

$$I_{DC} = I_{REF2} = \frac{k'_p}{2} \cdot \left(\frac{W}{L}\right)_C (V_{SGC} + V_{TP})^2$$

or

$$250 = \frac{40}{2}(15)[V_{SGC} + (-0.6)]^2 = 300(V_{SGC} - 0.6)^2$$

Then

$$V_{SGC} = \sqrt{\frac{250}{300}} + 0.6$$

or

$$V_{SGC} = 1.513 \text{ V}$$

Since $V_{SGC} = V_{SGB} = 1.513$ V, we obtain

$$I_B = I_{Q2} = \frac{k'_p}{2} \cdot \left(\frac{W}{L}\right)_B (V_{SGB} + V_{TP})^2$$

or

$$150 = \frac{40}{2} \cdot \left(\frac{W}{L}\right)_B [1.513 + (-0.6)]^2$$

V^+ V_{SGC} V_{SGB} M_C M_B I_{Q2} V_{SGA} M_A V_{SDA} I_{REF2} $R_D = 8$ kΩ V^-

(b)

We find

$$\left(\frac{W}{L}\right)_B = 9$$

For M_A, we have

$$I_{DA} = I_{Q2} = \frac{k'_p}{2} \cdot \left(\frac{W}{L}\right)_A (V_{SGA} + V_{TP})^2$$

or

$$150 = \frac{40}{2}(25)(V_{SGA} + (-0.6))^2 = 500(V_{SGA} - 0.6)^2$$

Now

$$V_{SGA} = \sqrt{\frac{150}{500}} + 0.6$$

or

$$V_{SGA} = 1.148 \text{ V}$$

The source-to-drain voltage of M_A is found from

$$V_{SDA} = V_{SGA} - I_{Q2}R_D - V^- = 1.148 - (0.15)(8) - (-3)$$

or

$$V_{SDA} = 2.95 \text{ V}$$

We may note that the transistor M_A is biased in the saturation region.

Comment: By designing the W/L ratios of the current mirror transistors, we can obtain different reference current and bias current values.

Constant-Current Biasing

$$K_{n3}(V_{GS3} - V_{TN3})^2 = K_{n4}(V_{GS4} - V_{TN4})^2$$

$$V_{GS4} + V_{GS3} = -V^-$$

$$V_{GS3} = \frac{-V^- - V_{TN4} + V_{TN3}\sqrt{K_{n3}/K_{n4}}}{1 + \sqrt{K_{n3}/K_{n4}}}$$

$$I_Q = K_{n2}(V_{GS3} - V_{TN2})^2$$

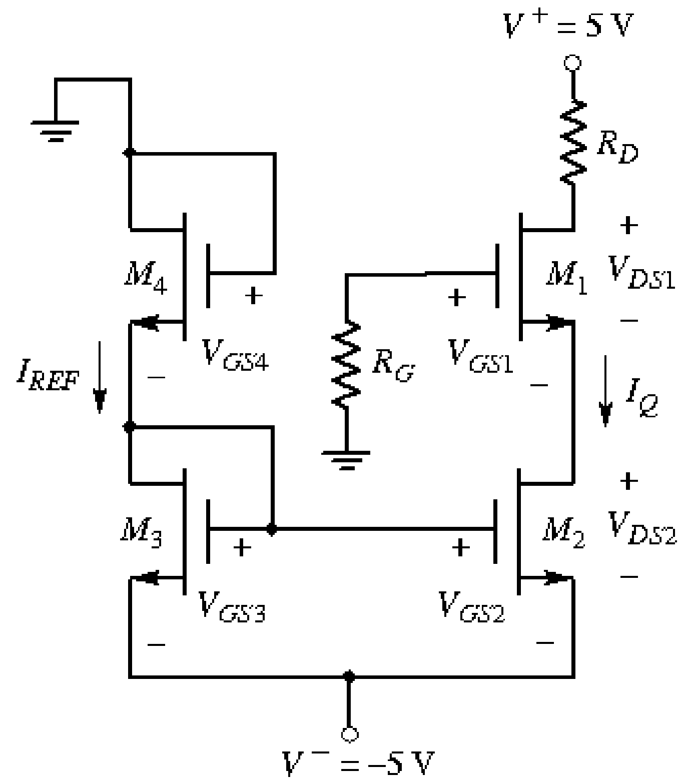


Figure 5.43 Implementation of a MOSFET constant-current source

Example 5.13 **Objective:** Determine the currents and voltages in a MOSFET constant-current source.

For the circuit shown in Figure 5.43, the transistor parameters are: $K_{n1} = 0.2\,\text{mA/V}^2$, $K_{n2} = K_{n3} = K_{n4} = 0.1\,\text{mA/V}^2$, and $V_{TN1} = V_{TN2} = V_{TN3} = V_{TN4} = 1\,\text{V}$.

Solution: From Equation (5.26), we can determine V_{GS3}, as follows:

$$V_{GS3} = \frac{\sqrt{\frac{0.1}{0.1}}[5-1]+1}{1+\sqrt{\frac{0.1}{0.1}}} = 2.5\,\text{V}$$

Since M_3 and M_4 are identical transistors, V_{GS3} should be one-half of the bias voltage. The bias current I_Q is then

$$I_Q = (0.1)\cdot(2.5-1)^2 = 0.225\,\text{mA}$$

The gate-to-source voltage on M_1 is found from

$$I_Q = K_{n1}(V_{GS1} - V_{TN1})^2$$

or

$$0.225 = (0.2)\cdot(V_{GS1}-1)^2$$

which yields

$$V_{GS1} = 2.06\,\text{V}$$

The drain-to-source voltage on M_2 is

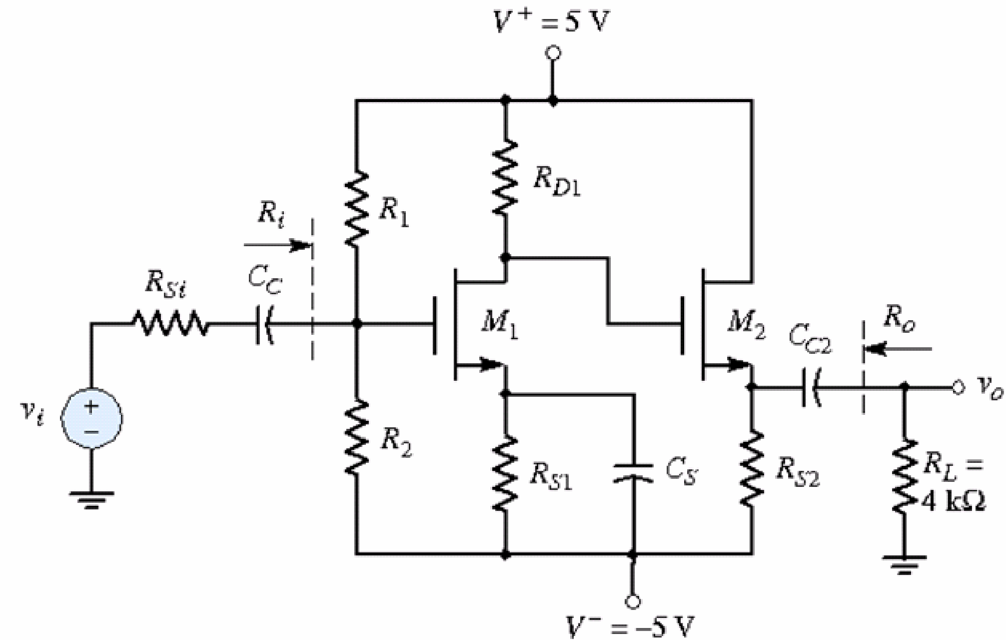
$$V_{DS2} = (-V^-) - V_{GS1} = 5 - 2.06 = 2.94\,\text{V}$$

Since $V_{DS2} = 2.94\,\text{V} > V_{DS}(\text{sat}) = V_{GS2} - V_{TN2} = 2.5 - 1 = 1.5\,\text{V}$, M_2 is biased in the saturation region.

Multitransistor Circuit: Cascade Configuration

Design Example 6.14 **Objective:** Design the biasing of a multistage MOSFET circuit to meet specific requirements.

Consider the circuit shown in Figure 6.49 with transistor parameters $K_{n1} = 500\,\mu A/V^2$, $K_{n2} = 200\,\mu A/V^2$, $V_{TN1} = V_{TN2} = 1.2\,V$, and $\lambda_1 = \lambda_2 = 0$. Design the circuit such that $I_{DQ1} = 0.2\,mA$, $I_{DQ2} = 0.5\,mA$, $V_{DSQ1} = V_{DSQ2} = 6\,V$, and $R_i = 100\,k\Omega$. Let $R_{Si} = 4\,k\Omega$.



Solution: For output transistor M_2, we have

$$V_{DSQ2} = 5 - (-5) - I_{DQ2}R_{S2}$$

or

$$6 = 10 - (0.5)R_{S2}$$

which yields $R_{S2} = 8\,k\Omega$. Also,

$$I_{DQ2} = K_{n2}(V_{GS2} - V_{TN2})^2$$

or

$$0.5 = 0.2(V_{GS2} - 1.2)^2$$

which yields

$$V_{GS2} = 2.78\,V$$

Since $V_{DSQ2} = 6\,V$, the source voltage of M_2 is $V_{S2} = -1\,V$. With $V_{GS2} = 2.78\,V$, the gate voltage on M_2 must be

$$V_{G2} = -1 + 2.78 = 1.78\,V$$

The resistor R_{D1} is then

$$R_{D1} = \frac{5 - 1.78}{0.2} = 16.1\,k\Omega$$

For $V_{DSQ1} = 6\,V$, the source voltage of M_1 is

$$V_{S1} = 1.78 - 6 = -4.22\,V$$

The resistor R_{S1} is then

$$R_{S1} = \frac{-4.22 - (-5)}{0.2} = 3.9\,\text{k}\Omega$$

For transistor M_1, we have

$$I_{DQ1} = K_{n1}(V_{GS1} - V_{TN1})^2$$

or

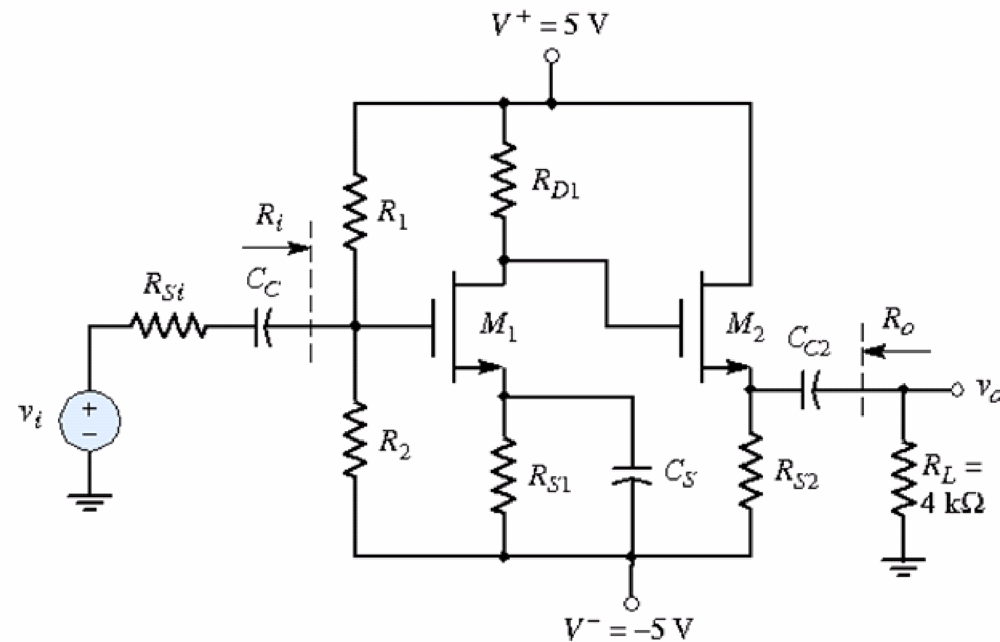
$$0.2 = 0.50(V_{GS1} - 1.2)^2$$

which yields

$$V_{GS1} = 1.83\,\text{V}$$

To find R_1 and R_2, we can write

$$V_{GS1} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - I_{DQ1}R_{S1}$$



Since

$$\frac{R_2}{R_1 + R_2} = \frac{1}{R_1} \cdot \left(\frac{R_1 R_2}{R_1 + R_2}\right) = \frac{1}{R_1} \cdot R_i$$

then

$$1.83 = \frac{1}{R_1}(100)(10) - (0.2)(3.9)$$

which yields $R_1 = 383\,\text{k}\Omega$. From $R_i = 100\,\text{k}\Omega$, we find that $R_2 = 135\,\text{k}\Omega$.

Multitransistor Circuit: Cascode Configuration

DESIGN EXAMPLE 3.21

Objective: Design the biasing of the cascode circuit to meet specific requirements.

For the circuit shown in Figure 3.57, the transistor parameters are: $V_{TN1} = V_{TN2} = 1.2$ V, $K_{n1} = K_{n2} = 0.8$ mA/V^2, and $\lambda_1 = \lambda_2 = 0$. Let $R_1 + R_2 + R_3 = 300$ kΩ and $R_S = 10$ kΩ. Design the circuit such that $I_{DQ} = 0.4$ mA and $V_{DSQ1} = V_{DSQ2} = 2.5$ V.

Solution: The dc voltage at the source of M_1 is

$$V_{S1} = I_{DQ}R_S - 5 = (0.4)(10) - 5 = -1 \text{ V}$$

Since M_1 and M_2 are identical transistors, and since the same current exists in the two transistors, the gate-to-source voltage is the same for both devices. We have

$$I_D = K_n(V_{GS} - V_{TN})^2$$

or

$$0.4 = 0.8(V_{GS} - 1.2)^2$$

which yields

$$V_{GS} = 1.907 \text{ V}$$

Then,

$$V_{G1} = \left(\frac{R_3}{R_1 + R_2 + R_3}\right)(5) = V_{GS} + V_{S1}$$

or

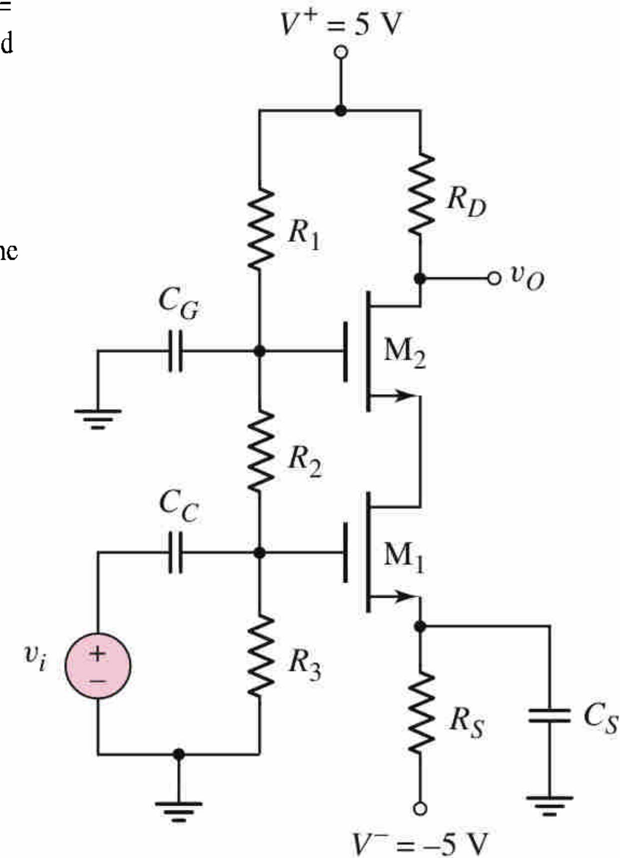
$$\left(\frac{R_3}{300}\right)(5) = 1.907 - 1 = 0.907$$

which yields

$$R_3 = 54.4 \text{ k}\Omega$$

The voltage at the source of M_2 is

$$V_{S2} = V_{DSQ1} + V_{S1} = 2.5 - 1 = 1.5 \text{ V}$$



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Then,

$$V_{G2} = \left(\frac{R_2 + R_3}{R_1 + R_2 + R_3}\right)(5) = V_{GS} + V_{S2}$$

or

$$\left(\frac{R_2 + R_3}{300}\right)(5) = 1.907 + 1.5 = 3.407 \text{ V}$$

which yields

$$R_2 + R_3 = 204.4 \text{ k}\Omega$$

and

$$R_2 = 150 \text{ k}\Omega$$

Therefore

$$R_1 = 95.6 \text{ k}\Omega$$

The voltage at the drain of M_2 is

$$V_{D2} = V_{DSQ2} + V_{S2} = 2.5 + 1.5 = 4 \text{ V}$$

The drain resistor is therefore

$$R_D = \frac{5 - V_{D2}}{I_{DQ}} = \frac{5 - 4}{0.4} = 2.5 \text{ k}\Omega$$

Comment: Since $V_{DS} = 2.5 \text{ V} > V_{GS} - V_{TN} = 1.91 - 1.2 = 0.71 \text{ V}$, each transistor is biased in the saturation region.

PN Junction Field-Effect Transistor

- Cross Section Structure

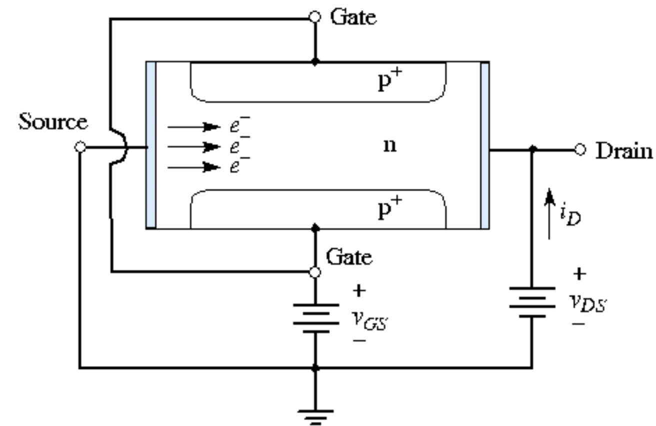
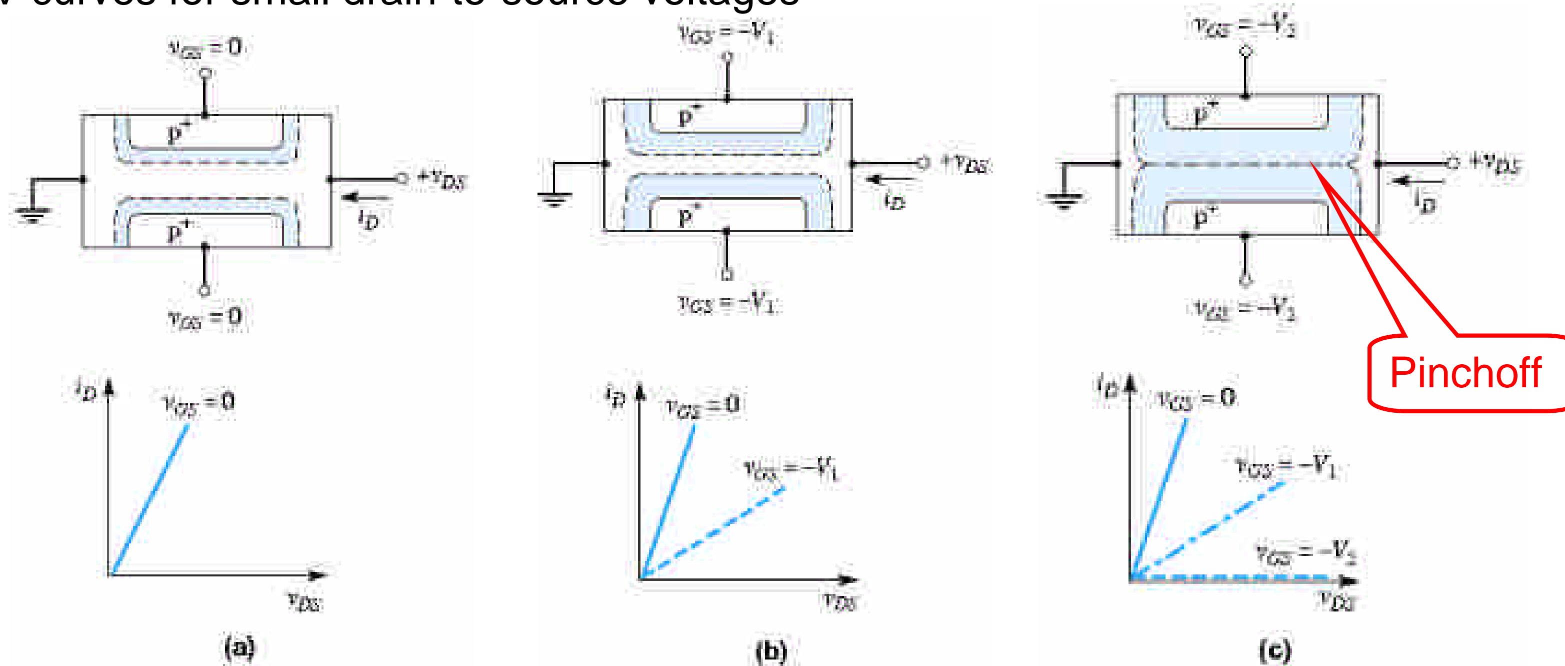


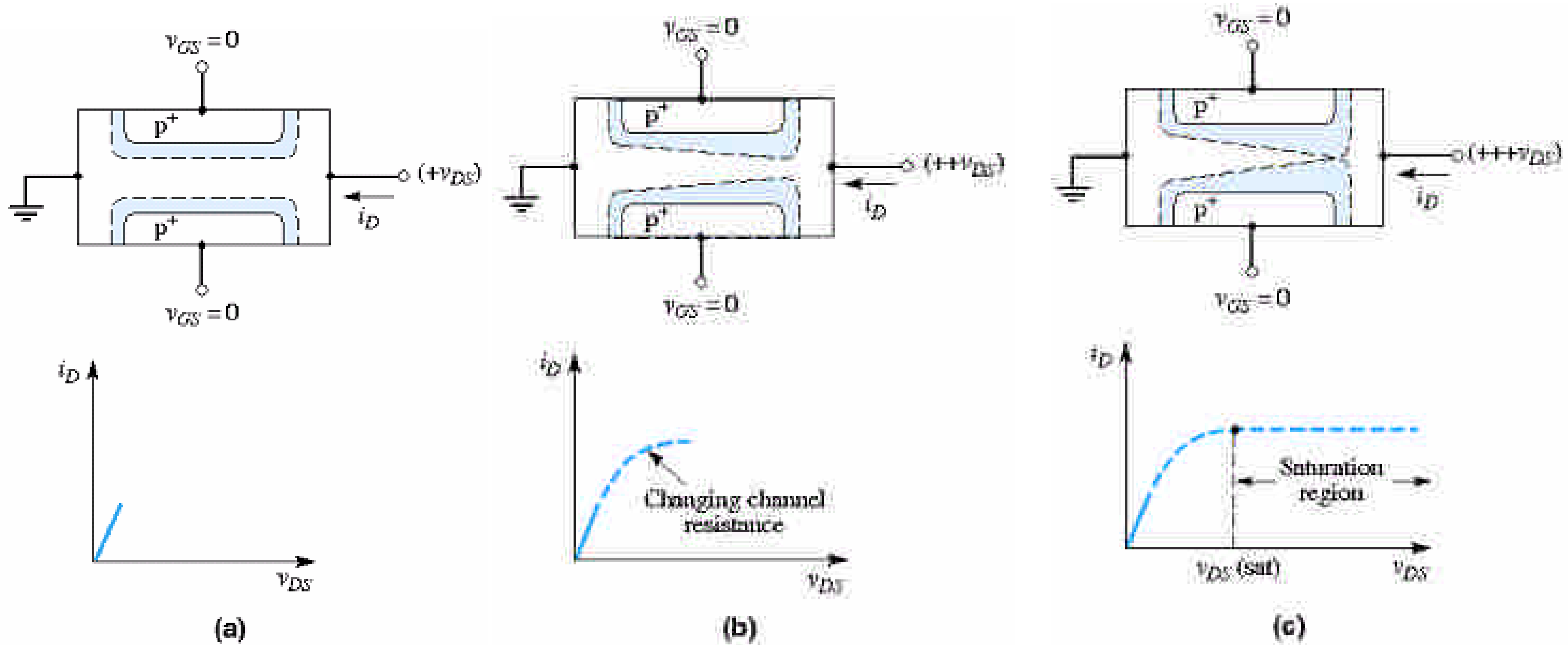
Figure 5.48 Cross section of a symmetrical n-channel pn junction field-effect transistor

- IV curves for small drain-to-source voltages



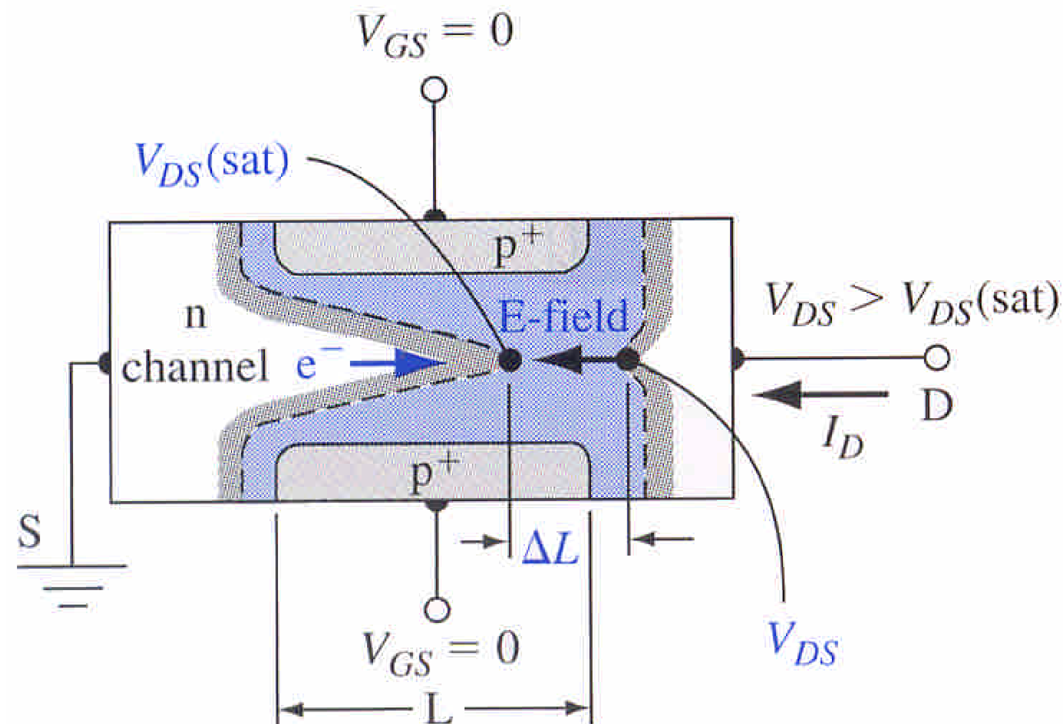
PN JFET

- The drain voltage changes for a given gate voltage.



Saturation Region in PN JFET

- If we assume that $\Delta L << L$, then the electronic field in the n-channel region remains unchanged from the $V_{DS(Sat)}$ case; the drain current will remain constant as V_{DS} changes.
- The electrons move through the n-channel from the source and are injected into the space charge region where, subjected to the E-field force, they are swept through into the drain contact area.



N-Channel Depletion-mode MESFET

- A reverse-bias gate-to-source voltage induces a space-charge region under the metal gate, which modulates the channel conductance.
- If a negative applied gate voltage is sufficiently large, the space-charge region will eventually reach the substrate, the pinchoff will occur.
- It is equivalent to an n-channel depletion-mode device, since a gate voltage must be applied to pinch off the channel.

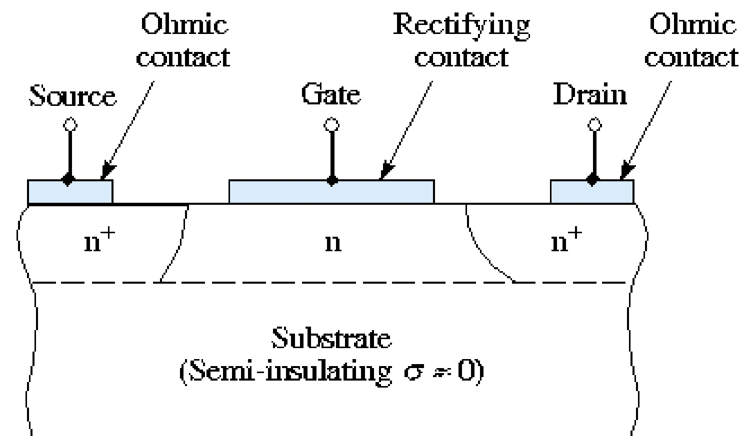


Figure 5.51 Cross section of an n-channel MESFET with a semi-insulating substrate

N-Channel Enhancement-mode MESFET

- The channel is pinched off even at $v_{GS} = 0$.
- To open the channel, the depletion region must be reduced; that is, a forward-biased voltage is applied to the gate-semiconductor (G-S) junction.
- The threshold voltage is the gate-to-source voltage required to create the pinch-off condition.

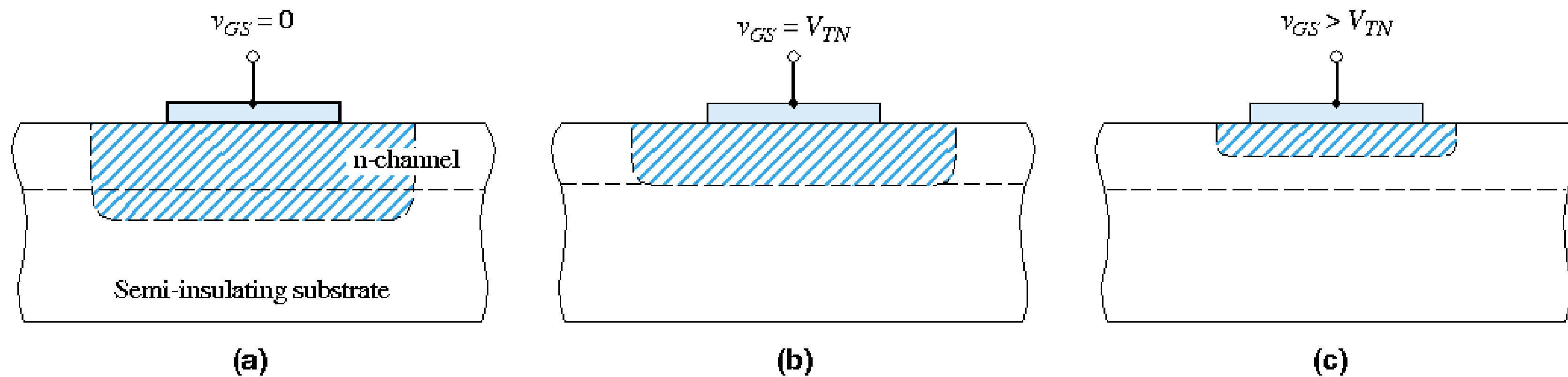
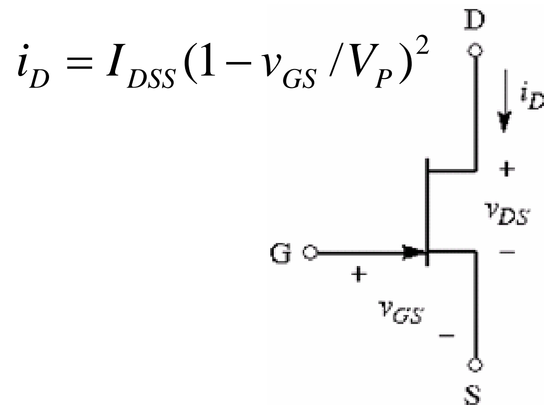
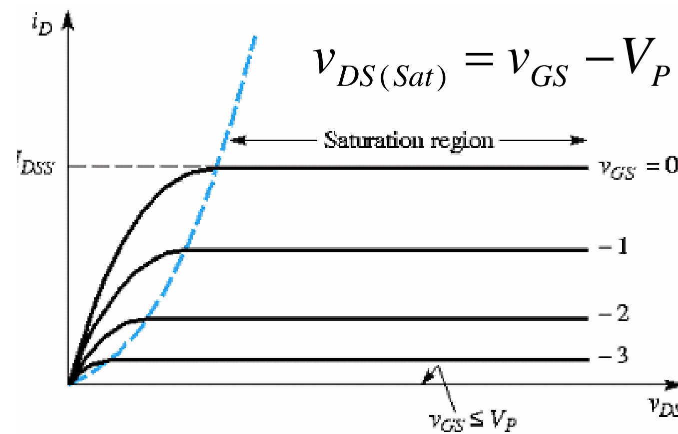


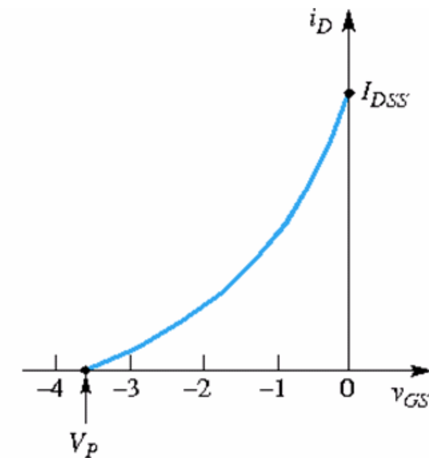
Figure 5.52 Channel space-charge region of an enhancement-mode MESFET for: (a) $v_{GS} = 0$, (b) $v_{GS} = V_{TN}$, and (c) $v_{GS} > V_{TN}$

Current-Voltage Characteristics

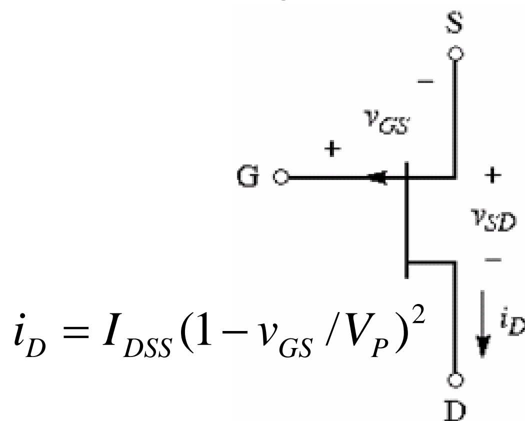
- N-channel JFET
  - ✓ The pinchoff voltage V_P for the n-channel JFET is negative and the gate-to-source voltage is usually negative; therefore, the ratio v_{GS}/V_P is positive.

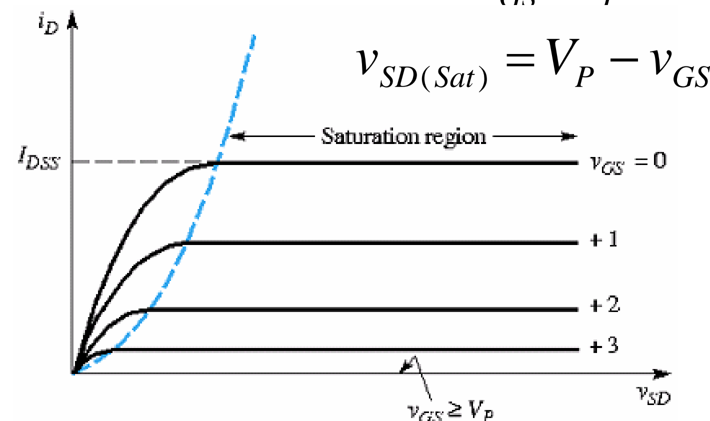


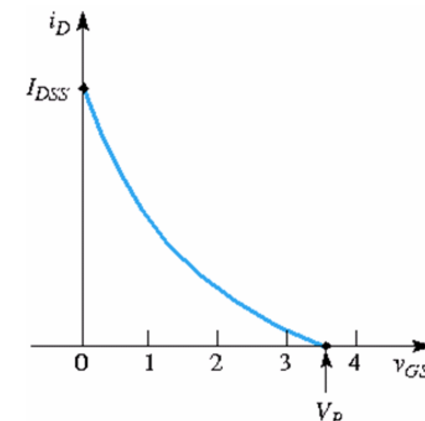




- P-channel JFET
  - ✓ The pinchoff voltage V_P for the n-channel JFET is positive and the gate-to-source voltage is usually positive; therefore, the ratio v_{GS}/V_P is positive.





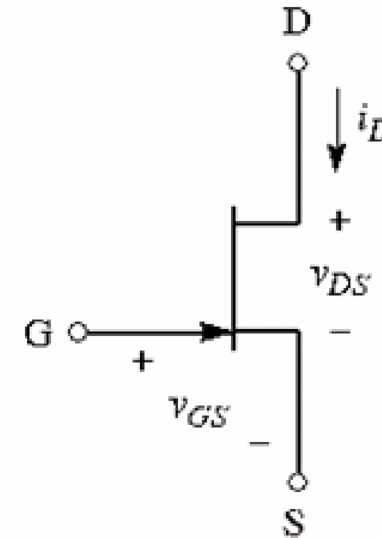


Example 5.16 **Objective:** Calculate i_D and $v_{DS}(\text{sat})$ in an n-channel pn JFET.

Assume the saturation current is $I_{DSS} = 2\,\text{mA}$ and the pinchoff voltage is $V_P = -3.5\,\text{V}$. Calculate i_D and $v_{DS}(\text{sat})$ for $v_{GS} = 0$, $V_P/4$, and $V_P/2$.

Solution: From Equation (5.30), we have

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 = (2)\left(1 - \frac{v_{GS}}{(-3.5)}\right)^2$$



Therefore, for $v_{GS} = 0$, $V_P/4$, and $V_P/2$, we obtain

$$i_D = 2, 1.13, \text{ and } 0.5\,\text{mA}$$

From Equation (5.31), we have

$$v_{DS}(\text{sat}) = v_{GS} - V_P = v_{GS} - (-3.5)$$

Therefore, for $v_{GS} = 0$, $V_P/4$, and $V_P/2$, we obtain

$$v_{DS}(\text{sat}) = 3.5, 2.63, \text{ and } 1.75\,\text{V}$$

JFET Properties

- Output Resistance for PN JFET

$$i_D = I_{DSS}(1 - v_{GS}/V_P)^2(1 + \lambda v_{DS})$$

$$r_O = \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Bigg|_{v_{GS}=\text{const.}} = \left[\lambda I_{DSS}(1 - v_{GS}/V_P)^2 \right]^{-1} \approx \left[\lambda I_{DQ} \right]^{-1}$$

- Saturation Region for Ideal Enhancement-mode MESFET

$$i_D = K_n(v_{GS} - V_{TN})^2$$

For an n-channel enhancement-mode MESFET, the threshold voltage is positive.

- Nonsaturation Region for Ideal Enhancement-mode MESFET

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$$

Design Example 5.17 **Objective:** Design the dc bias of a JFET circuit with an n-channel depletion-mode JFET.

For the circuit in Figure 5.56(a), the transistor parameters are: $I_{DSS} = 5\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $I_D = 2\,\text{mA}$ and $V_{DS} = 6\,\text{V}$.

Solution: Assume the transistor is biased in the saturation region. The dc drain current is then given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or

$$2 = 5\left(1 - \frac{V_{GS}}{(-4)}\right)^2$$

Therefore,

$$V_{GS} = -1.47\,\text{V}$$

From Figure 5.56(b) we see that the current through the source resistor can be written as

$$I_D = \frac{-V_{GS}}{R_S}$$

Therefore,

$$R_S = \frac{-V_{GS}}{I_D} = \frac{-(-1.47)}{2} = 0.735\,\text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

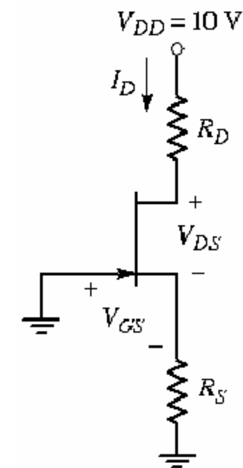
Therefore,

$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 6 - (2)(0.735)}{2} = 1.27\,\text{k}\Omega$$

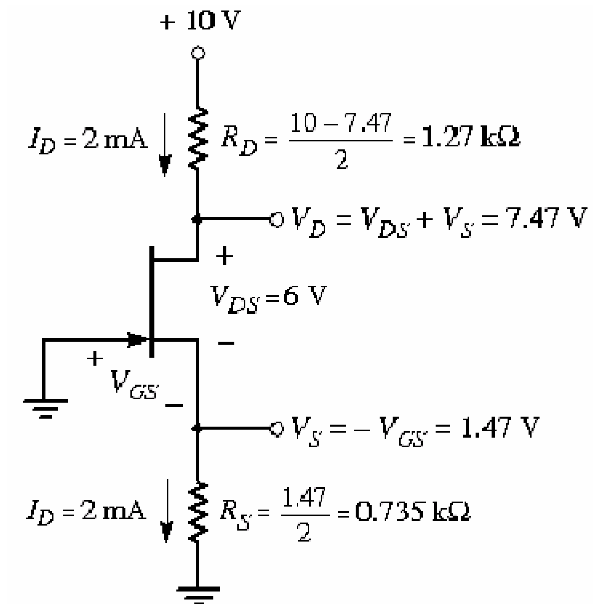
We also see that

$$V_{DS} = 6\,\text{V} > V_{GS} - V_P = -1.47 - (-4) = 2.53\,\text{V}$$

which shows that the JFET is indeed biased in the saturation region, as initially assumed.



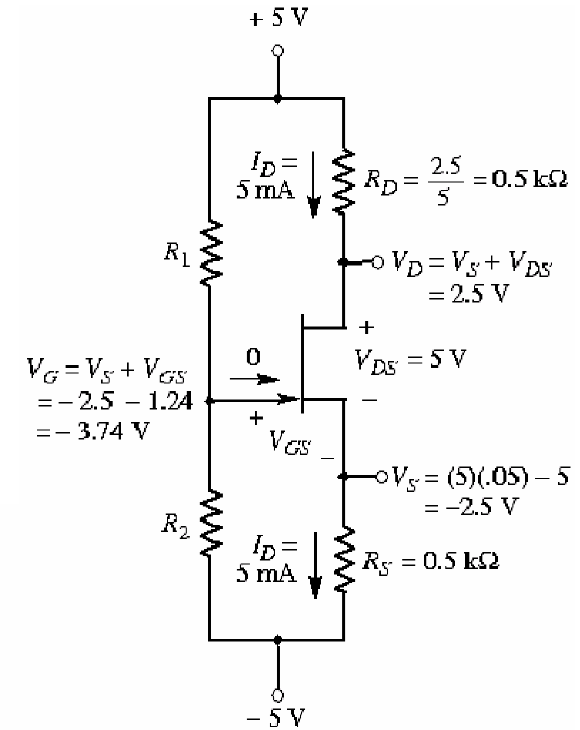
(a)



(b)

Design Example 5.18 **Objective:** Design a JFET circuit with a voltage divider biasing circuit.

Consider the circuit shown in Figure 5.57(a) with transistor parameters $I_{DSS} = 12\,\text{mA}$, $V_P = -3.5\,\text{V}$, and $\lambda = 0$. Let $R_1 + R_2 = 100\,\text{k}\Omega$. Design the circuit such that the dc drain current is $I_D = 5\,\text{mA}$ and the dc drain-to-source voltage is $V_{DS} = 5\,\text{V}$.



Solution: Assume the transistor is biased in the saturation region. The dc drain current is then given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Therefore,

$$5 = 12\left(1 - \frac{V_{GS}}{(-3.5)}\right)^2$$

which yields

$$V_{GS} = -1.24\,\text{V}$$

From Figure 5.57(b), the voltage at the source terminal is

$$V_S = I_D R_S - 5 = (5)(0.5) - 5 = -2.5\,\text{V}$$

which means that the gate voltage is

$$V_G = V_{GS} + V_S = -1.24 - 2.5 = -3.74\,\text{V}$$

We can also write the gate voltage as

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5$$

or

$$-3.74 = \frac{R_2}{100}(10) - 5 \cdot$$

Therefore,

$$R_2 = 12.6\,\text{k}\Omega$$

and

$$R_1 = 87.4\,\text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = 5 - I_D R_D - I_D R_S - (-5)$$

Therefore,

$$R_D = \frac{10 - V_{DS} - I_D R_S}{I_D} = \frac{10 - 5 - (5)(0.5)}{5} = 0.5\,\text{k}\Omega$$

We also see that

$$V_{DS} = 5\,\text{V} > V_{GS} - V_P = -1.24 - (-3.5) = 2.26\,\text{V}$$

which shows that the JFET is indeed biased in the saturation region, as initially assumed.

Comment: The dc analysis of the JFET circuit is essentially the same as that of the MOSFET circuit, since the gate current is assumed to be zero.

Example 5.19 **Objective:** Calculate the quiescent current and voltage values in a p-channel JFET circuit.

The parameters of the transistor in the circuit shown in Figure 5.58 are: $I_{DSS} = 2.5\,\text{mA}$, $V_P = +2.5\,\text{V}$, and $\lambda = 0$. The transistor is biased with a constant- current source.

Solution: From Figure 5.58, we can write the dc drain current as

$$I_D = I_Q = 0.8\,\text{mA} = \frac{V_D - (-9)}{R_D}$$

which yields

$$V_D = (0.8)(4) - 9 = -5.8\,\text{V}$$

Now, assume the transistor is biased in the saturation region. We then have

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or

$$0.8 = 2.5\left(1 - \frac{V_{GS}}{2.5}\right)^2$$

which yields

$$V_{GS} = 1.086\,\text{V}$$

Then

$$V_S = 1 - V_{GS} = 1 - 1.086 = -0.086\,\text{V}$$

and

$$V_{SD} = V_S - V_D = -0.086 - (-5.8) = 5.71\,\text{V}$$

Again, we see that

$$V_{SD} = 5.71\,\text{V} > V_P - V_{GS} = 2.5 - 1.086 = 1.41\,\text{V}$$

which verifies that the transistor is biased in the saturation region, as assumed.

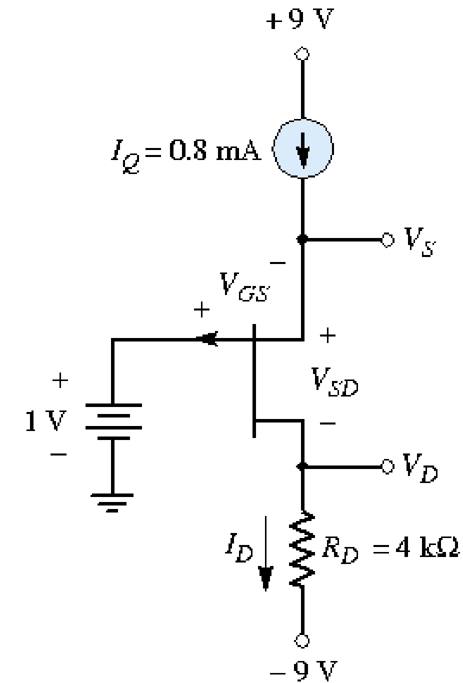


Figure 5.58 A p-channel JFET circuit biased with a constant-current source

Design Example 5.20 Objective: Design a circuit with an enhancement-mode MESFET.

Consider the circuit shown in Figure 5.59(a). The transistor parameters are: $V_{TN} = 0.24\,\text{V}$, $K_n = 1.1\,\text{mA/V}^2$, and $\lambda = 0$. Let $R_1 + R_2 = 50\,\text{k}\Omega$. Design the circuit such that $V_{GS} = 0.50\,\text{V}$ and $V_{DS} = 2.5\,\text{V}$.

Solution: From Equation (5.36(a)) the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = (1.1)(0.5 - 0.24)^2 = 74.4\,\mu\text{A}$$

From Figure 5.59(b), the voltage at the drain is

$$V_D = V_{DD} - I_D R_D = 4 - (0.0744)(6.7) = 3.5\,\text{V}$$

Therefore, the voltage at the source is

$$V_S = V_D - V_{DS} = 3.5 - 2.5 = 1\,\text{V}$$

The source resistance is then

$$R_S = \frac{V_S}{I_D} = \frac{1}{0.0744} = 13.4\,\text{k}\Omega$$

The voltage at the gate is

$$V_G = V_{GS} + V_S = 0.5 + 1 = 1.5\,\text{V}$$

Since the gate current is zero, the gate voltage is also given by a voltage divider equation, as follows:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

or

$$1.5 = \left(\frac{R_2}{50}\right)(4)$$

which yields

$$R_2 = 18.75\,\text{k}\Omega$$

and

$$R_1 = 31.25\,\text{k}\Omega$$

Again, we see that

$$V_{DS} = 2.5\,\text{V} > V_{GS} - V_{TN} = 0.5 - 0.24 = 0.26\,\text{V}$$

which confirms that the transistor is biased in the saturation region, as initially assumed.