# Basic FET Amplifiers

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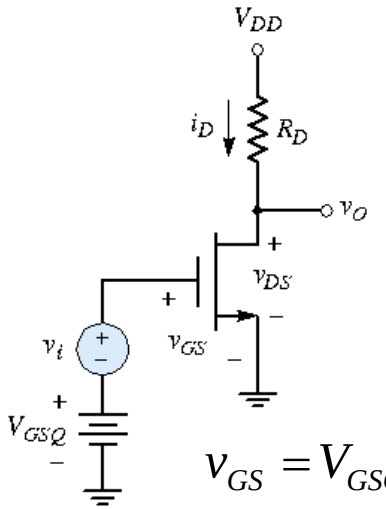
# Small-Signal Model for MOSFETs

$$
\begin{aligned}
i_D &= K_n(v_{GS} - V_{TN})^2 \\
&= K_n(V_{GSQ} + v_{gs} - V_{TN})^2 \\
&= K_n[(V_{GSQ} - V_{TN}) + v_{gs}]^2 \\
&= K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} + K_n v_{gs}^2 \\
&\approx K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} \\
&= I_{DQ} + i_d \qquad \text{if } v_{gs} << 2(V_{GSQ} - V_{TN})
\end{aligned}
$$

$$
\begin{aligned}
g_m &= \frac{i_d}{v_{gs}} \\
&= 2K_n(V_{GSQ} - V_{TN}) \\
&= 2\sqrt{K_n I_{DQ}}
\end{aligned}
$$




$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs}$$

**Figure 6.1** NMOS common-source circuit with time-varying signal source in series with gate dc source

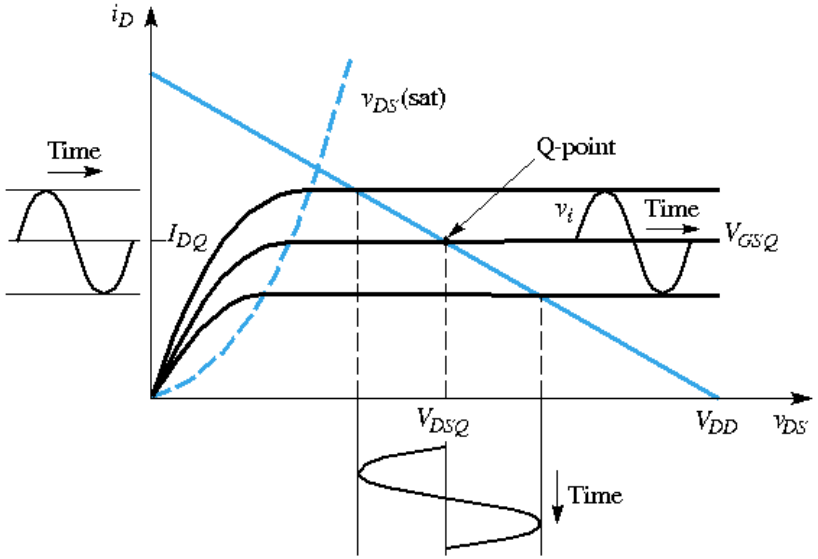



**Figure 6.2** Common-source transistor characteristics, dc load line, and sinusoidal variation in gate-to-source voltage, drain current, and drain-to-source voltage

# Transconductance for MOSFETs

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GSQ}} = 2\sqrt{K_n I_{DQ}}$$

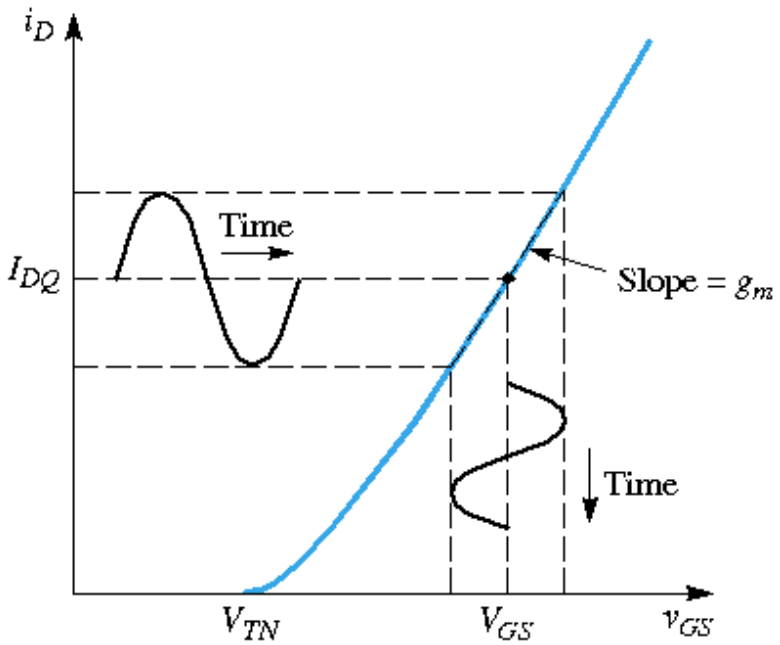



**Figure 6.3** Drain current versus gate-to-source voltage characteristics, with superimposed sinusoidal signals

**Example 6.1** **Objective:** Calculate the transconductance of an n-channel MOSFET.

Consider an n-channel MOSFET with parameters $V_{TN} = 1\,\text{V}$, $\left(\frac{1}{2}\right)\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, and $W/L = 40$. Assume the drain current is $I_D = 1\,\text{mA}$.

**Solution:** The conduction parameter is

$$K_n = \left(\frac{1}{2}\mu_n C_{ox}\right)\left(\frac{W}{L}\right) = (20)(40)\,\mu\text{A/V}^2 \Rightarrow 0.80\,\text{mA/V}^2$$

Assuming the transistor is biased in the saturation region, the transconductance is determined from Equation (6.8(b)),

$$g_m = 2\sqrt{K_n I_{DQ}} = 2\sqrt{(0.8)(1)} = 1.79\,\text{mA/V}$$

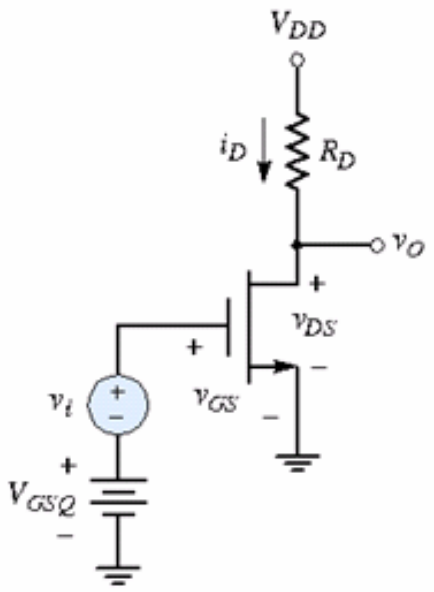
**Comment:** The transconductance of a bipolar transistor is $g_m = (I_{CQ}/V_T)$, which is 38.5 mA/V for a collector current of 1 mA. The transconductance values of MOSFETs tend to be small compared to those of BJTs. However, the advantages of MOSFETs include high input impedance, small size, and low power dissipation.

# AC Equivalent Circuit for MOSFETs

$$v_O = V_{DD} - i_D R_D$$
$$= V_{DD} - (I_{DQ} + i_d) R_D$$
$$= (V_{DD} - I_{DD} R_D) - i_D R_D$$
$$= V_O + v_o$$

$$v_o = -i_d R_D$$

$$i_d = g_m v_{gs} = g_m v_i$$



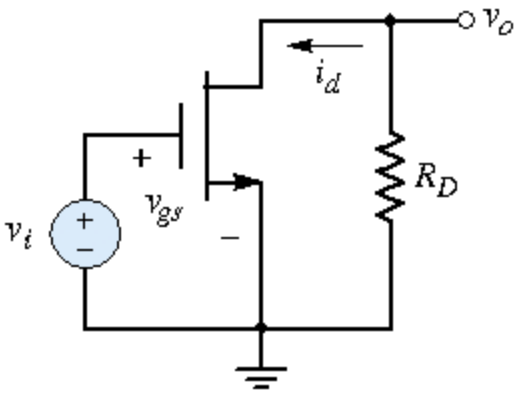




**Figure 6.4** AC equivalent circuit of common-source amplifier with NMOS transistor

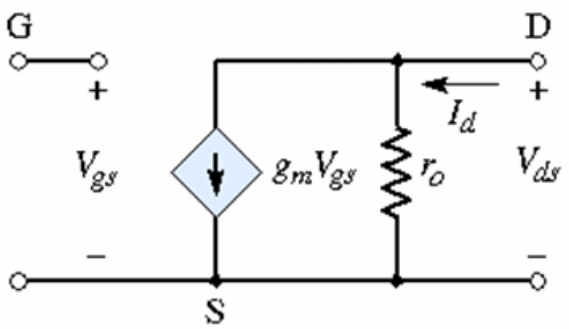
# Small-Signal Equivalent Circuit for MOSFETs

- Finite Output Resistance

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})]$$

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=V_{GSQ}}$$

$$= [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \approx [\lambda I_{DQ}]^{-1}$$



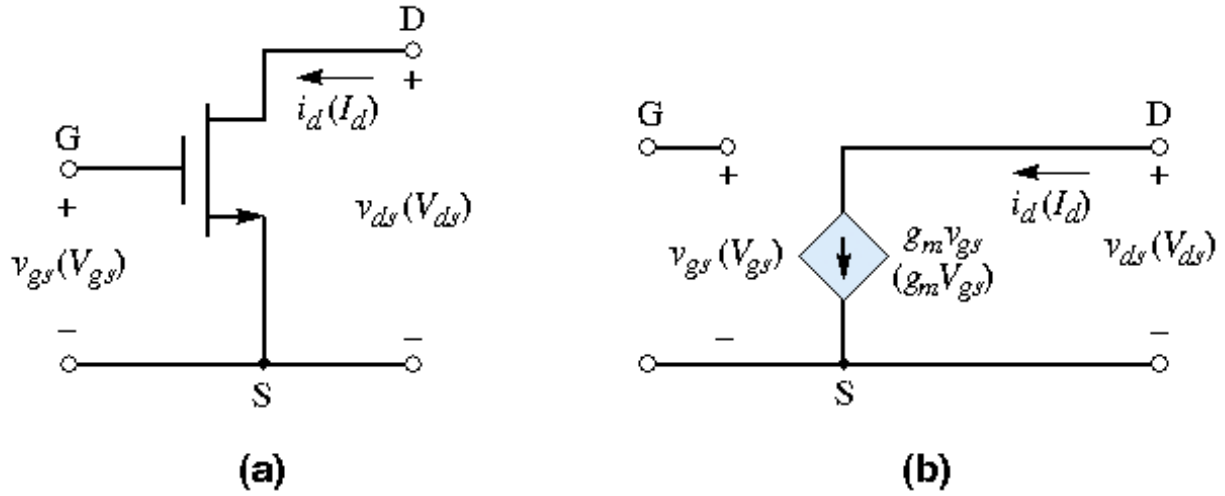
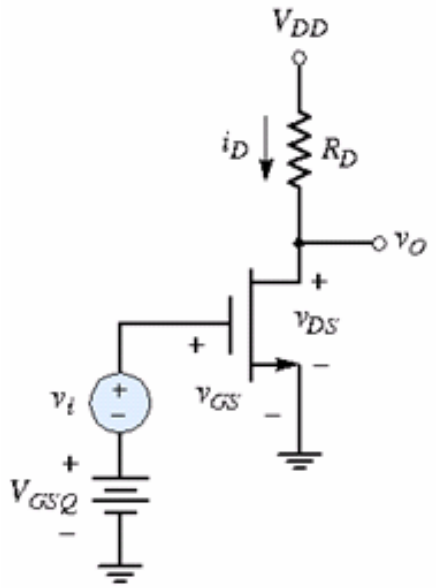




**Figure 6.5** (a) Common-source NMOS transistor with small-signal parameters and (b) simplified small-signal equivalent circuit for NMOS transistor

**Example 6.2** **Objective:** Determine the small-signal voltage gain of a MOSFET circuit.

For the circuit in Figure 6.1, assume parameters are: $V_{GSQ} = 2.12\,\text{V}$, $V_{DD} = 5\,\text{V}$, and $R_D = 2.5\,\text{k}\Omega$. Assume transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 0.80\,\text{mA/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Assume the transistor is biased in the saturation region.




**Solution:** The quiescent values are

$$I_{DQ} \cong K_n(V_{GSQ} - V_{TN})^2 = (0.8)(2.12 - 1)^2 = 1.0\,\text{mA}$$

and

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 5 - (1)(2.5) = 2.5\,\text{V}$$

Therefore,

$$V_{DSQ} = 2.5\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 1.82 - 1 = 0.82\,\text{V}$$

which means that the transistor is biased in the saturation region, as initially assumed, and as required for a linear amplifier. The transconductance is

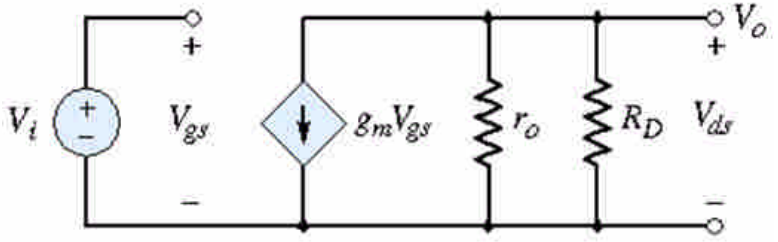
$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.8)(2.12 - 1) = 1.79\,\text{mA/V}$$

and the output resistance is

$$r_o = [\lambda I_{DQ}]^{-1} = [(0.02)(1)]^{-1} = 50\,\text{k}\Omega$$

From Figure 6.7, the output voltage is

$$V_o = -g_m V_{gs}(r_o \| R_D)$$




Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_d) = -(1.79)(50 \| 2.5) = -4.26$$

# PMOS Common-Source Circuits

$$V_o = g_m V_{sg}(r_o \,//\, R_D)$$

$$V_{sg} = -V_i$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \,//\, R_D)$$

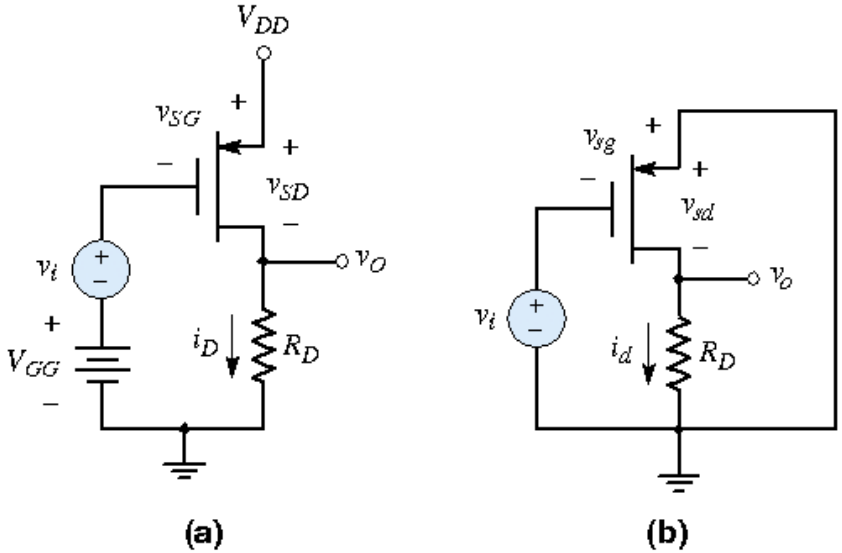



**Figure 6.8** (a) Common-source circuit with PMOS transistor and (b) corresponding ac equivalent circuit

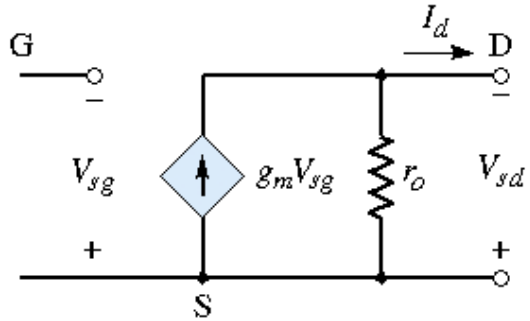



**Figure 6.9** Small-signal equivalent circuit of PMOS transistor

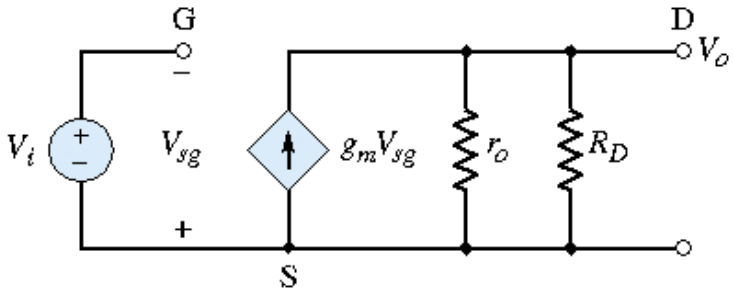



**Figure 6.10** Small-signal equivalent circuit of common-source amplifier with PMOS transistor model

# Modeling the Body Effect

$$i_D = K_n(v_{GS} - V_{TN})^2$$

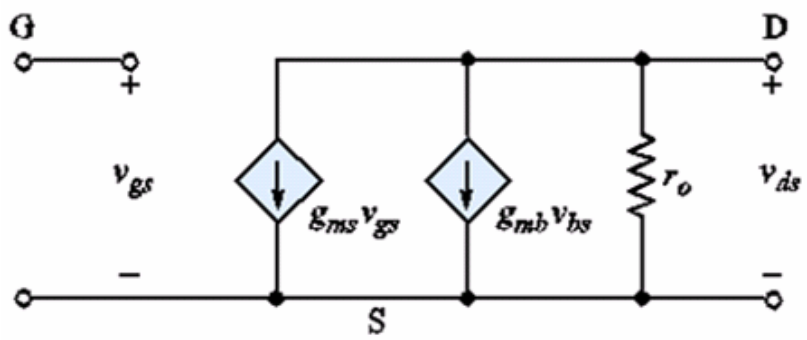
$$V_{TN} = V_{TNO} + \gamma[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}]$$

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \left.\frac{-\partial i_D}{\partial v_{SB}}\right|_Q = -\frac{\partial i_D}{\partial V_{TN}}\frac{\partial V_{TN}}{\partial v_{SB}}\bigg|_Q$$

$$\frac{\partial i_D}{\partial V_{TN}} = -2K_n(v_{GS} - V_{TN}) = -g_m$$

$$\frac{\partial V_{TN}}{\partial v_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + v_{SB}}} \equiv \eta$$

$$g_{mb} = -(-g_m)\eta = g_m\eta$$



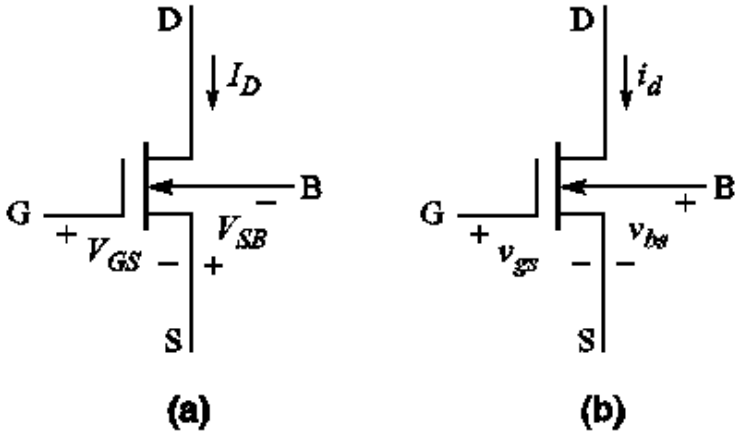




**Figure 6.11** The four-terminal NMOS device with (a) dc voltages and (b) ac voltages

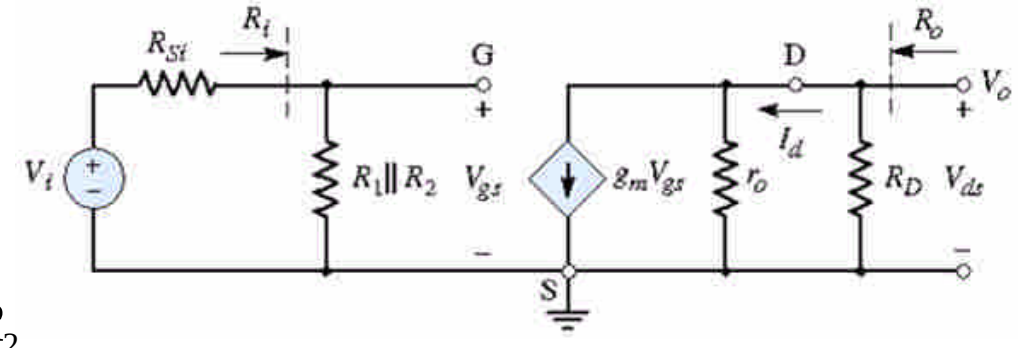
# The Common-Source Amplifier

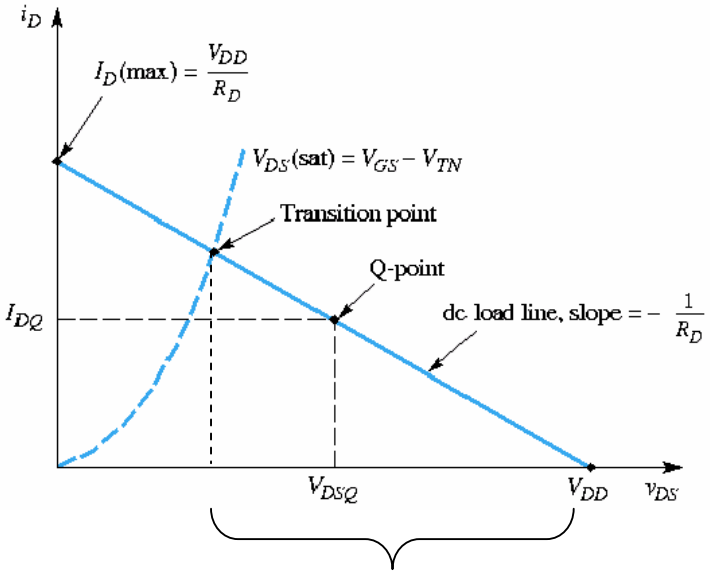
- Assume that the transistor is biased in the saturation region and that the signal frequency is sufficiently large for the coupling capacitor to act essentially as a short circuit.

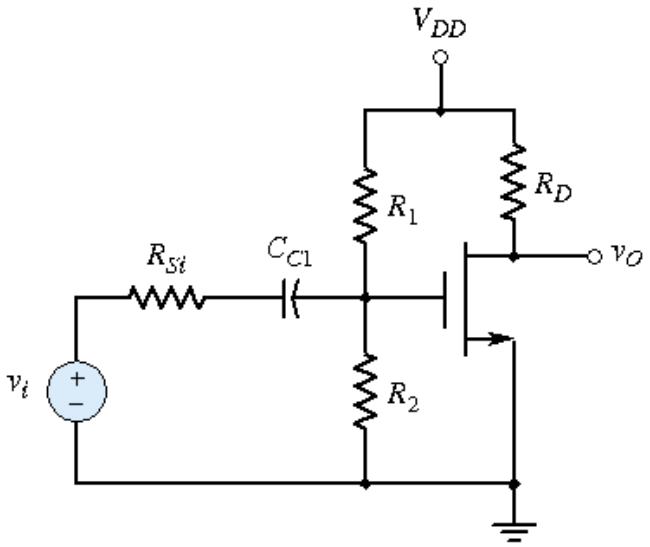
$$V_o = -g_m V_{gs}(r_o \,//\, R_D)$$

$$V_{gs} = \frac{R_1 \,//\, R_2}{R_{Si} + R_1 \,//\, R_2} V_i$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \,//\, R_D)\frac{R_1 \,//\, R_2}{R_{Si} + R_1 \,//\, R_2}$$




Input Resistance

$$R_i = R_1 \,//\, R_2$$

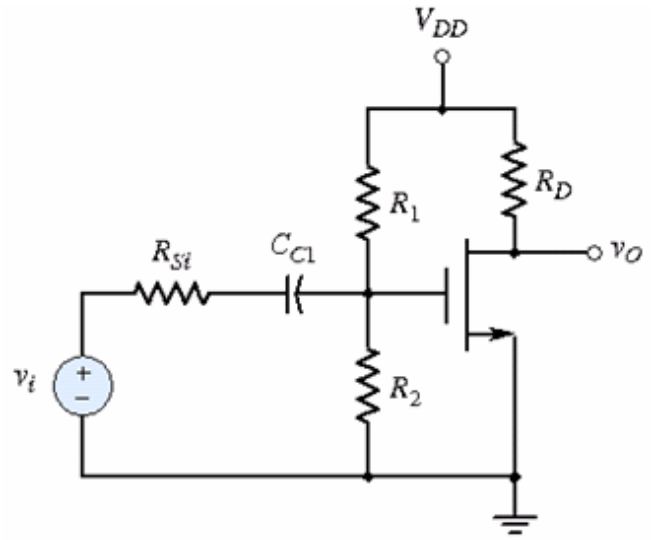
Output Resistance

$$R_o = R_D \,//\, r_o$$

**Figure 6.13** Common-source circuit with voltage divider biasing and coupling capacitor

**Example 6.3** **Objective:** Determine the small-signal voltage gain and input and output resistances of a common-source amplifier.

For the circuit shown in Figure 6.13, the parameters are: $V_{DD} = 10\,\text{V}$, $R_1 = 70.9\,\text{k}\Omega$, $R_2 = 29.1\,\text{k}\Omega$, and $R_D = 5\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 1.5\,\text{V}$, $K_n = 0.5\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. Assume $R_{Si} = 4\,\text{k}\Omega$.




**Solution:** **DC Calculations**: The dc or quiescent gate-to-source voltage is

$$V_{GSQ} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{29.1}{70.9 + 29.1}\right)(10) = 2.91\,\text{V}$$

The quiescent drain current is

$$I_{DQ} = K_n(V_{GSQ} - V_{TN})^2 = (0.5)(2.91 - 1.5)^2 = 1\,\text{mA}$$

and the quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 10 - (1)(5) = 5\,\text{V}$$

Since $V_{DSQ} > V_{GSQ} - V_{TN}$, the transistor is biased in the saturation region.

**Small-signal Voltage Gain:** The small-signal transconductance $g_m$ is then

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.5)(2.91 - 1.5) = 1.41\,\text{mA/V}$$

and the small-signal output resistance $r_o$ is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(1)]^{-1} = 100\,\text{k}\Omega$$

The amplifier input resistance is

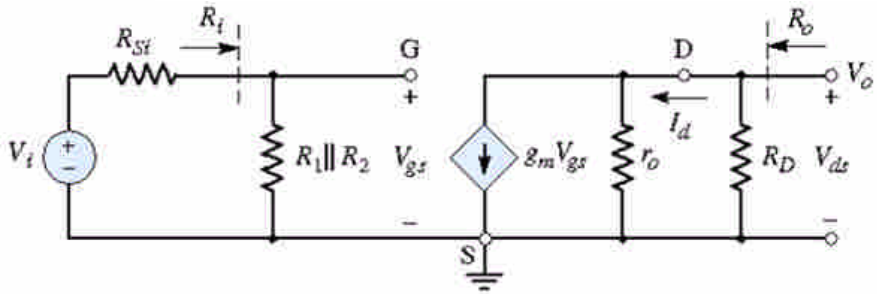
$$R_i = R_1 \| R_2 = 70.9 \| 29.1 = 20.6\,\text{k}\Omega$$

From Figure 6.14 and Equation (6.29), the small-signal voltage gain is

$$A_v = -g_m(r_o \| R_D) \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) = -(1.41)(100 \| 5)\left(\frac{20.6}{20.6 + 4}\right)$$

or

$$A_v = -5.62$$




**Input and Output Resistances:** As already calculated, the amplifier input resistance is

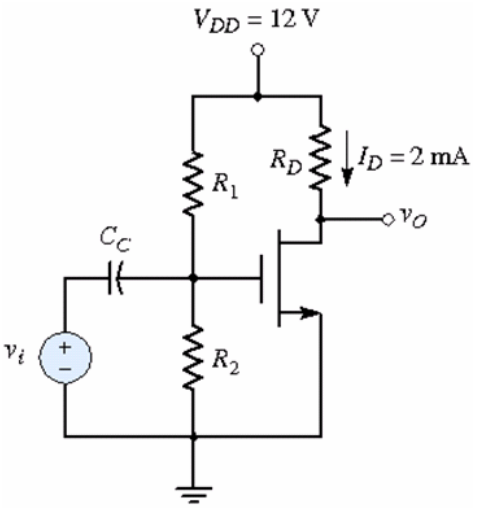
$$R_i = R_1 \| R_2 = 70.9 \| 29.1 = 20.6\,\text{k}\Omega$$

and the amplifier output resistance is

$$R_o = R_D \| r_o = 5 \| 100 = 4.76\,\text{k}\Omega$$

**Design Example 6.4** **Objective:** Design the bias of a MOSFET such that the $Q$-point is in the middle of the saturation region.

Consider the circuit in Figure 6.16 with transistor parameters $V_{TN} = 1\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0.015\,\text{V}^{-1}$. Let $R_i = R_1 \| R_2 = 100\,\text{k}\Omega$. Design the circuit such that $I_{DQ} = 2\,\text{mA}$ and the $Q$-point is in the middle of the saturation region.




**Solution:** The load line and the desired $Q$-point are given in Figure 6.17. If the $Q$-point is to be in the middle of the saturation region, the current at the transition point must be 4 mA.

We can now calculate $V_{DS}(\text{sat})$ at the transition point. The subscript $t$ indicates transition point values. To determine $V_{GSt}$, we use

$$I_{Dt} = 4 = K_n(V_{GSt} - V_{TN})^2 = 1(V_{GSt} - 1)^2$$

which yields

$$V_{GSt} = 3\,\text{V}$$

Therefore

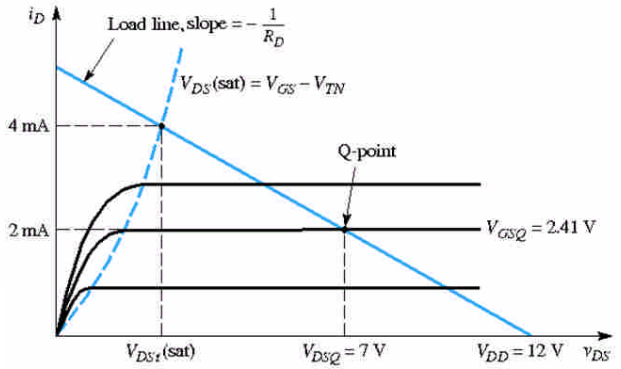
$$V_{DSt} = V_{GSt} - V_{TN} = 3 - 1 = 2\,\text{V}$$

If the $Q$-point is in the middle of the saturation region, then $V_{DSQ} = 7\,\text{V}$, which would yield a 10 V peak-to-peak symmetrical output voltage. From Figure 6.16, we can write

$$V_{DSQ} = V_{DD} - I_{DQ}R_D$$

or

$$R_D = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} = \frac{12 - 7}{2} = 2.5\,\text{k}\Omega$$



We can determine the required quiescent gate-to-source voltage from the current equation, as follows:

$$I_{DQ} = 2 = K_n(V_{GSQ} - V_{TN})^2 = (1)(V_{GSQ} - 1)^2$$

or

$$V_{GSQ} = 2.41\,\text{V}$$

Then

$$V_{GSQ} = 2.41 = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{1}{R_1}\right)\left(\frac{R_1 R_2}{R_1 + R_2}\right)(V_{DD})$$
$$= \frac{R_i}{R_1} \cdot V_{DD} = \frac{(100)(12)}{R_1}$$

which yields

$$R_1 = 498\,\text{k}\Omega \quad \text{and} \quad R_2 = 125\,\text{k}\Omega$$

We can then determine the small-signal equivalent circuit parameters from the $Q$-point values. The transconductance is $g_m = 2.82\,\text{mA/V}$, the transistor output resistance is $r_o = 33.3\,\text{k}\Omega$, and the small-signal voltage gain, assuming an ideal signal source, is

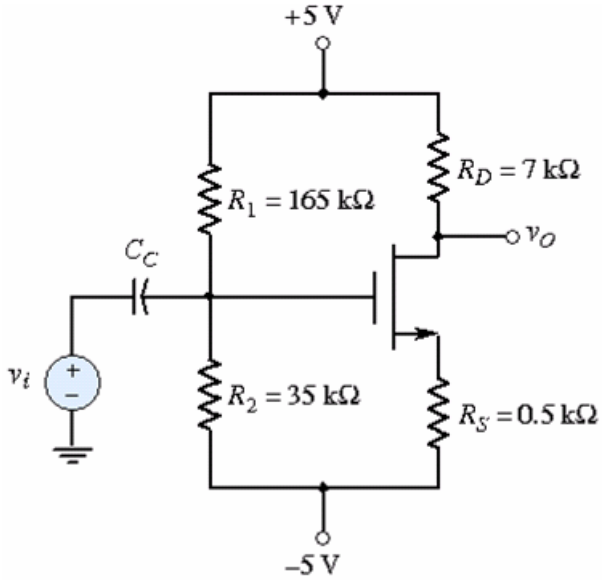
$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D) = -(2.82)(33.3 \| 2.5) = -6.56$$

**Comment:** Establishing the $Q$-point in the middle of the saturation region allows the maximum symmetrical swing in the output voltage, while keeping the transistor biased in the saturation region.

# Common-Source Amplifier with Source Resistor

**Example 6.5** **Objective:** Determine the small-signal voltage gain of a common-source circuit containing a source resistor.

Consider the circuit in Figure 6.18. The transistor parameters are $V_{TN} = 0.8\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$.




**Solution:** From the dc analysis of the circuit, we find that $V_{GSQ} = 1.50\,\text{V}$, $I_{DQ} = 0.50\,\text{mA}$, and $V_{DSQ} = 6.25\,\text{V}$. The small-signal transconductance is

$$g_m = 2K_n(V_{GS} - V_{TN}) = 2(1)(1.50 - 0.8) = 1.4\,\text{mA/V}$$

and the small-signal resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1} = \infty$$

The output voltage is

$$V_o = -g_m V_{gs} R_D$$

Writing a KVL equation from the input around the gate–source loop, we find

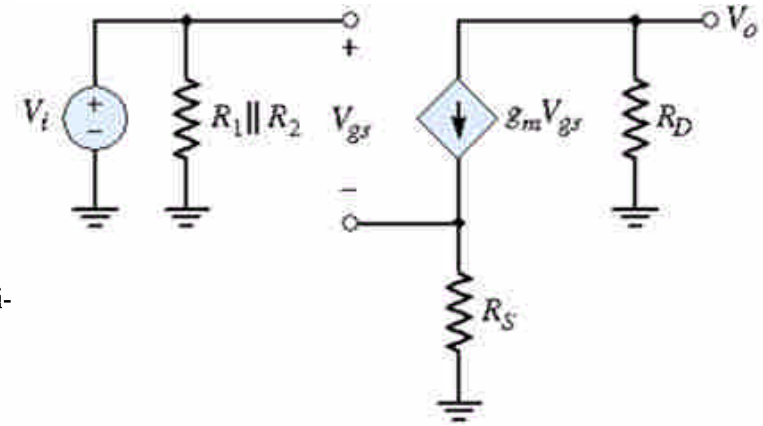
$$V_i = V_{gs} + (g_m V_{gs})R_S = V_{gs}(1 + g_m R_S)$$

or

$$V_{gs} = \frac{V_i}{1 + g_m R_S}$$

The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}$$




We may note that if $g_m$ were large, then the small-signal voltage gain would be approximately

$$A_v \cong \frac{-R_D}{R_S}$$

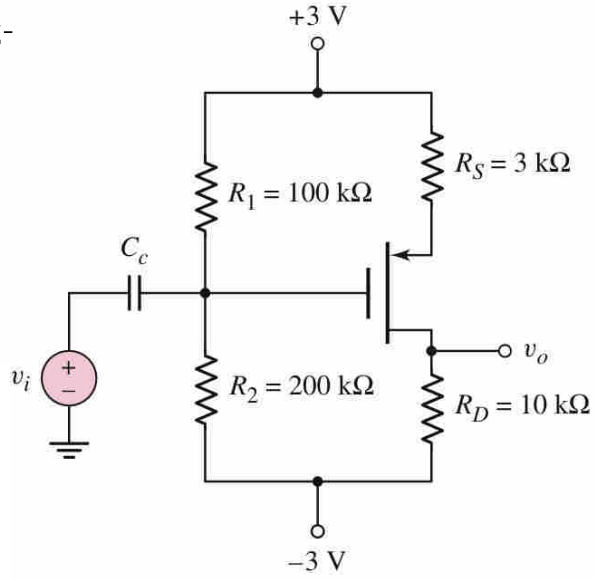
Substituting the appropriate parameters into the actual voltage gain expression, we find

$$A_v = \frac{-(1.4)(7)}{1 + (1.4)(0.5)} = -5.76$$

## EXAMPLE 4.6

**Objective:** Determine the small-signal voltage gain of a PMOS transistor circuit.

Consider the circuit shown in Figure 4.21(a). The transistor parameters are $K_p = 0.25$ mA/V$^2$, $V_{TP} = -0.5$ V, and $\lambda = 0$. The quiescent drain current is found to be $I_{DQ} = 0.20$ mA. The small-signal equivalent circuit is shown in Figure 4.21(b).




**Solution:** The small-signal output voltage is

$$V_o = +g_m V_{sg} R_D$$

Writing a KVL equation from the input around the gate–source loop, we find

$$V_i = -V_{sg} - g_m V_{sg} R_S$$

or

$$V_{sg} = \frac{-V_i}{1 + g_m R_S}$$

Substituting this expression for $V_{sg}$ into the output voltage equation, we small-signal voltage gain as

$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}$$

The small-signal transconductance is

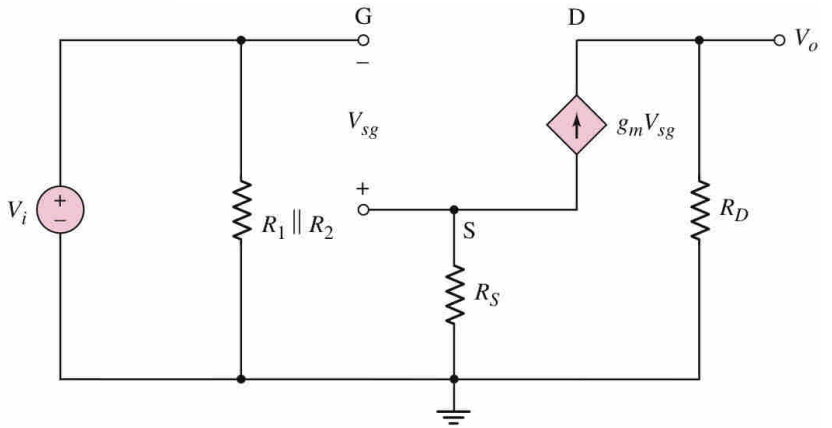
$$g_m = 2\sqrt{K_p I_{DQ}} = 2\sqrt{(0.25)(0.20)} = 0.447\,\text{mA/V}$$

We then find

$$A_v = \frac{-(0.447)(10)}{1 + (0.447)(3)}$$

or

$$A_v = -1.91$$



# Common-Source Circuit with Source Bypass Capacitor

**Example 6.6** **Objective:** Determine the small-signal voltage gain of a circuit biased with a constant-current source and incorporating a source bypass capacitor.

For the circuit shown in Figure 6.22, the transistor parameters are: $V_{TN} = 0.8\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$.

**Solution:** Since the dc gate current is zero, the dc voltage at the source terminal is $V_S = -V_{GSQ}$, and the gate-to-source voltage is determined from

$$I_{DQ} = I_Q = K_n(V_{GSQ} - V_{TN})^2$$

or

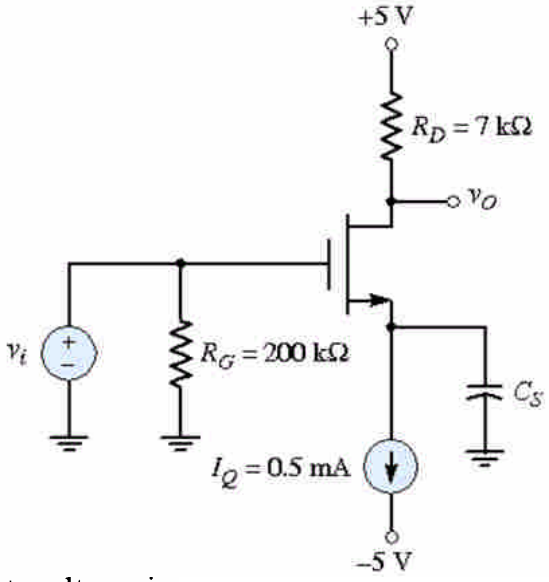
$$0.5 = (1)(V_{GSQ} - 0.8)^2$$

which yields

$$V_{GSQ} = -V_S = 1.51\,\text{V}$$

The quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ}R_D - V_S = 5 - (0.5)(7) - (-1.51) = 3.01\,\text{V}$$



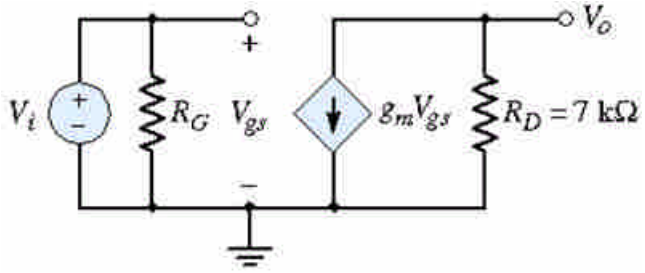

The transistor is therefore biased in the saturation region.

The small-signal equivalent circuit is shown in Figure 6.23. The output voltage is

$$V_o = -g_m V_{gs} R_D$$

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m R_D = -(1.4)(7) = -9.8$$



# The Source-Follower Amplifier

- Small-Signal Voltage Gain

$$V_o = g_m V_{gs}(R_S // r_o)$$

$$V_{gs} = \frac{R_i}{R_i + R_{si}} V_i - g_m V_{gs}(R_S // r_o)$$

$$V_{gs} = \frac{R_i /(R_i + R_{si})}{1 + g_m(R_S // r_o)} V_i$$

$$A_v = \frac{g_m(R_S // r_o)}{1 + g_m(R_S // r_o)} \frac{R_i}{R_i + R_{si}}$$

- Input Resistance

$$R_i = R_1 // R_2$$

- Output Resistance

$$I_x + g_m V_{gs} = V_x /(R_S // r_o)$$

$$I_x - g_m V_x = V_x /(R_S // r_o)$$

$$(g_m + \frac{1}{R_S} + \frac{1}{r_o})V_x = I_x$$

$$R_o = \frac{V_x}{I_x} = \frac{1}{g_m} // R_S // r_o$$

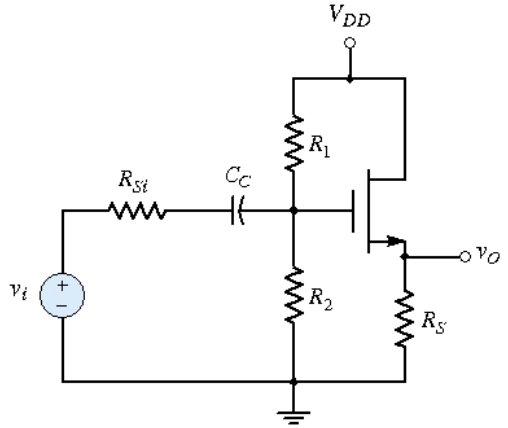
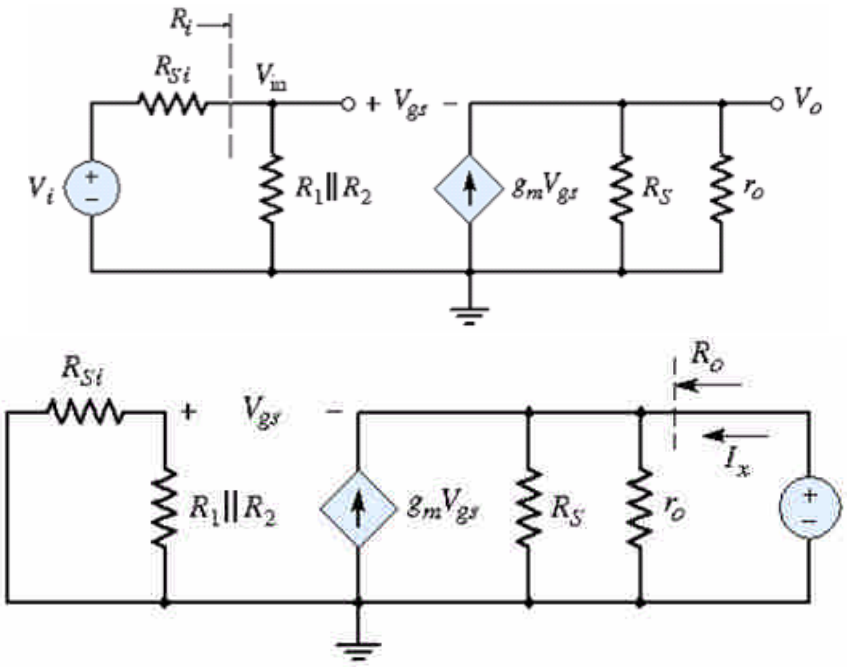



Figure 6.28 NMOS source-follower or common-drain amplifier



## EXAMPLE 4.8

**Objective:** Calculate the small-signal voltage gain of the source-follower circuit in Figure 4.30.

Assume the circuit parameters are $V_{DD} = 12$ V, $R_1 = 162$ kΩ, $R_2 = 463$ kΩ, and $R_S = 0.75$ kΩ, and the transistor parameters are $V_{TN} = 1.5$ V, $K_n = 4$ mA/V$^2$, and $\lambda = 0.01$ V$^{-1}$. Also assume $R_{Si} = 4$ kΩ.

**Solution:** The dc analysis results are $I_{DQ} = 7.97$ mA and $V_{GSQ} = 2.91$ V. The small-signal transconductance is therefore

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(4)(2.91 - 1.5) = 11.3 \text{ mA/V}$$

and the small-signal transistor resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(7.97)]^{-1} = 12.5\,\text{k}\Omega$$

The amplifier input resistance is

$$R_i = R_1 \| R_2 = 162 \| 463 = 120\,\text{k}\Omega$$

The small-signal voltage gain then becomes

$$A_v = \frac{g_m(R_S \| r_o)}{1 + g_m(R_S \| r_o)} \cdot \frac{R_i}{R_i + R_{Si}}$$

$$= \frac{(11.3)(0.75 \| 12.5)}{1 + (11.3)(0.75 \| 12.5)} \cdot \frac{120}{120 + 4} = +0.860$$

## DESIGN EXAMPLE **4.9**

**Objective:** Design a source-follower amplifier with a p-channel enhancement MOSFET to meet a set of specifications.

**Specifications:** The circuit to be designed has the configuration sho Figure 4.32 with circuit parameters $V_{DD} = 20$ V and $R_{Si} = 4$ kΩ. The $Q$-po ues are to be in the center of the load line with $I_{DQ} = 2.5$ mA. The input res is to be $R_i = 200$ kΩ. The transistor $W/L$ ratio is to be designed such that th signal voltage gain is $A_v = 0.90$.

**Choices:** A transistor with nominal parameters $V_{TP} = -2$ V, $k'_p = 40$ and $\lambda = 0$ is available. However, the tolerances in the $V_{TP}$ and $k'_p$ parame ±5 percent.

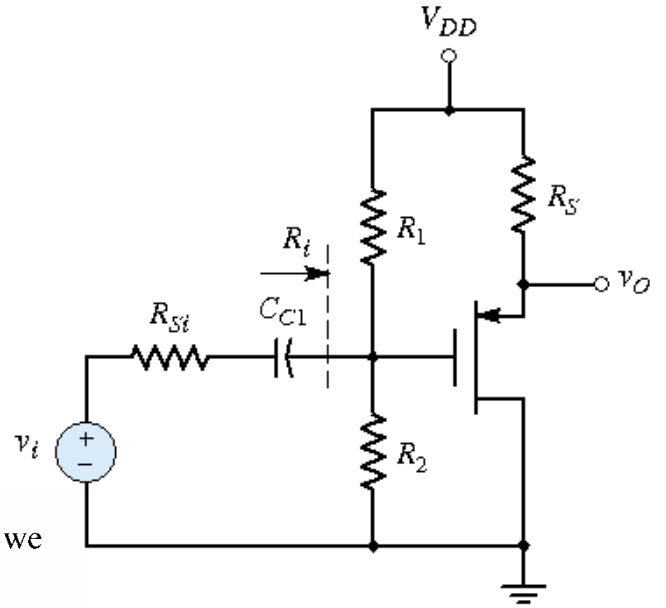



**Figure 6.30** PMOS source follower

**Solution (dc analysis):** From a KVL equation around the source-to-drain loop, we have

$$V_{DD} = V_{SDQ} + I_{DQ}R_S$$

or

$$20 = 10 + (2.5)R_S$$

which yields the required source resistor to be $R_S = 4$ kΩ.

**Solution (ac design):** The small-signal voltage gain of this circuit is the same as that of a source follower with an NMOS device. From Equation (4.33(a)), we have

$$A_v = \frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \cdot \frac{R_i}{R_i + R_{Si}}$$

which yields

$$0.90 = \frac{g_m(4)}{1 + g_m(4)} \cdot \frac{200}{200 + 4}$$

We find that the required transconductance must be $g_m = 2.80$ mA/V. The transconductance can be written as

$$g_m = 2\sqrt{K_p I_{DQ}}$$

We have

$$2.80 \times 10^{-3} = 2\sqrt{K_p(2.5 \times 10^{-3})}$$

which yields

$$K_p = 0.784 \times 10^{-3} \text{A/V}^2$$

The conduction parameter, as a function of width-to-length ratio, is

$$K_p = 0.784 \times 10^{-3} = \frac{k'_p}{2} \cdot \frac{W}{L} = \left(\frac{40 \times 10^{-6}}{2}\right) \cdot \left(\frac{W}{L}\right)$$

which means that the required width-to-length ratio must be

$$\frac{W}{L} = 39.2$$

**Solution (dc design):** Completing the dc analysis and design, we have

$$I_{DQ} = K_p(V_{GSQ} + V_{TP})^2$$

or

$$2.5 = 0.784(V_{SGQ} - 2)^2$$

which yields a quiescent source-to-gate voltage of $V_{SGQ} = 3.79$ V. The quiescent source-to-gate voltage can also be written as

$$V_{SGQ} = (V_{DD} - I_{DQ}R_S) - \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

Since

$$\left(\frac{R_2}{R_1 + R_2}\right) = \left(\frac{1}{R_1}\right)\left(\frac{R_1 R_2}{R_1 + R_2}\right) = \left(\frac{1}{R_1}\right) \cdot R_i$$

we have

$$3.79 = [20 - (2.5)(4)] - \left(\frac{1}{R_1}\right)(200)(20)$$

The bias resistor $R_1$ is then found to be

$$R_1 = 644\,\text{k}\Omega$$

Since $R_i = R_1 \| R_2 = 200\,\text{k}\Omega$, we find

$$R_2 = 290\,\text{k}\Omega$$

# Common-Gate Circuits

- Small-Signal Voltage Gain

$$V_O = -g_m V_{gs}(R_D \,//\, R_L)$$

$$V_i - (-V_{gs}) = R_{Si} I_i = R_{Si}(-g_m V_{gs})$$

$$V_{gs} = \frac{-V_i}{1 + g_m R_{Si}} \qquad A_v = \frac{g_m (R_D \,//\, R_L)}{1 + g_m R_{Si}}$$

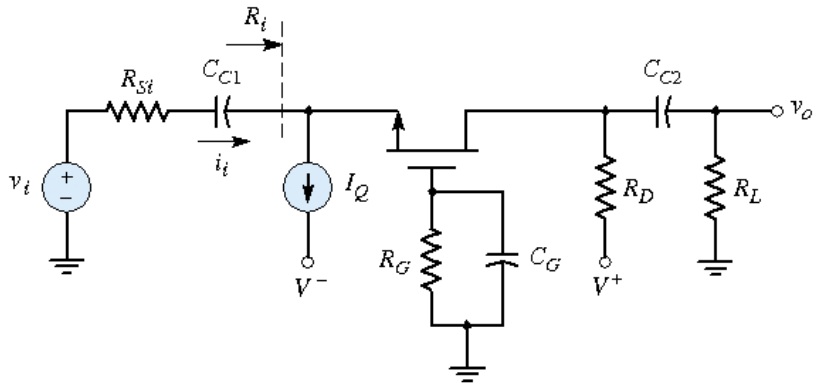


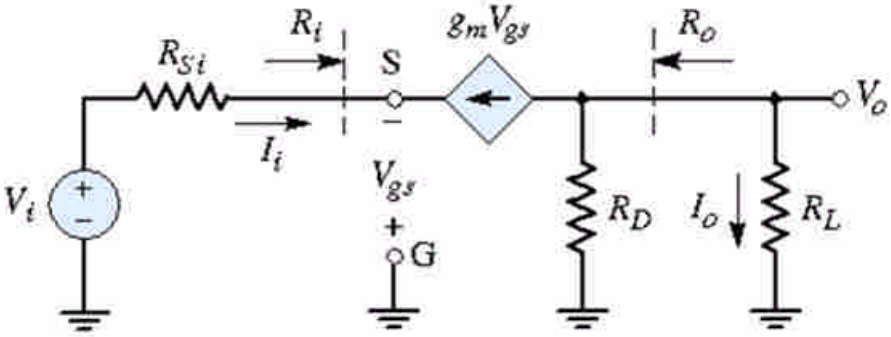

Figure 6.34 Common-gate circuit

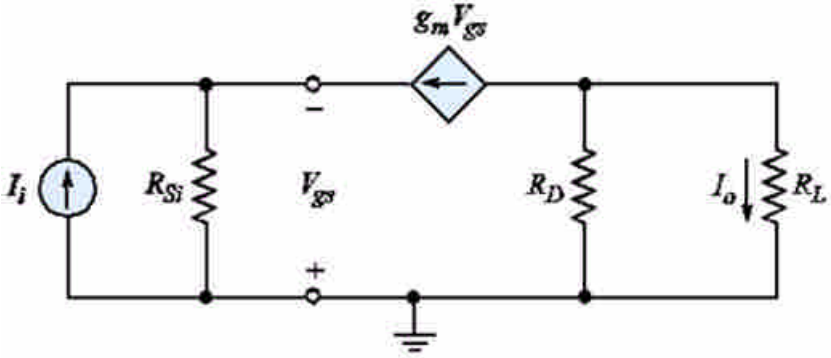
- Small-Signal Current Gain

$$I_O = \frac{-g_m V_{gs} R_D}{R_D + R_L}$$

$$I_i + g_m V_{gs} = \frac{-V_{gs}}{R_{Si}}, \quad I_i = \frac{-(1 + g_m R_{Si}) V_{gs}}{R_{Si}}$$

$$A_i = \frac{I_O}{I_i} = \frac{R_D}{R_D + R_L} \cdot \frac{g_m R_{Si}}{1 + g_m R_{Si}}$$




- Input and Output Resistance

$$R_i = \frac{-V_{gs}}{-g_m V_{gs}} = \frac{1}{g_m}, \quad R_O = R_D \quad (\because V_{gs} = 0)$$

**Example 6.10** **Objective:** For the common-gate circuit, determine the output voltage for a given input current.

For the circuits shown in Figures 6.34 and 6.36, the circuit parameters are: $I_Q = 1\,\text{mA}$, $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_G = 100\,\text{k}\Omega$, $R_D = 4\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$. Assume the input current is $100 \sin \omega t\,\mu\text{A}$ and assume $R_{Si} = 50\,\text{k}\Omega$.

**Solution:** The quiescent gate-to-source voltage is determined from

$$I_Q = I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$$

or

$$1 = 1(V_{GSQ} - 1)^2$$

which yields

$$V_{GSQ} = 2\,\text{V}$$

The small-signal transconductance is

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(1)(2 - 1) = 2\,\text{mA/V}$$

From Equation (6.45), we can write the output current as

$$I_o = I_i\left(\frac{R_D}{R_D + R_L}\right) \cdot \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right)$$

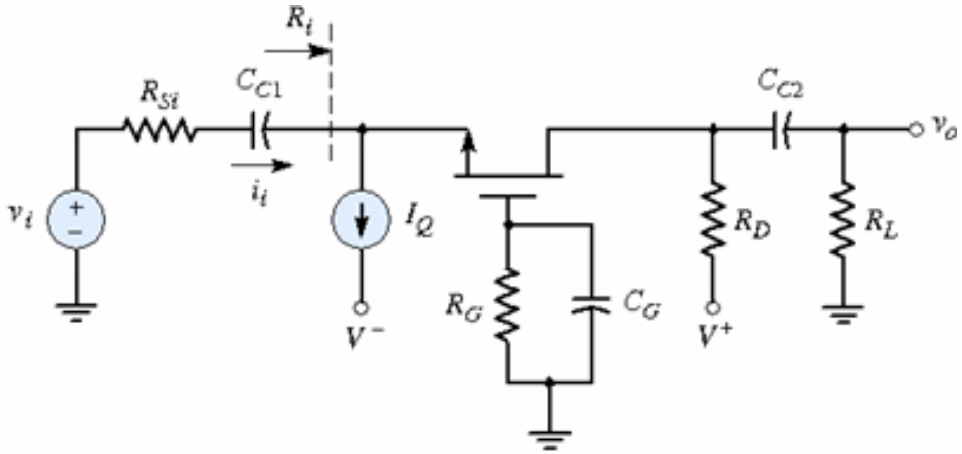
The output voltage is $V_o = I_o R_L$, so we find

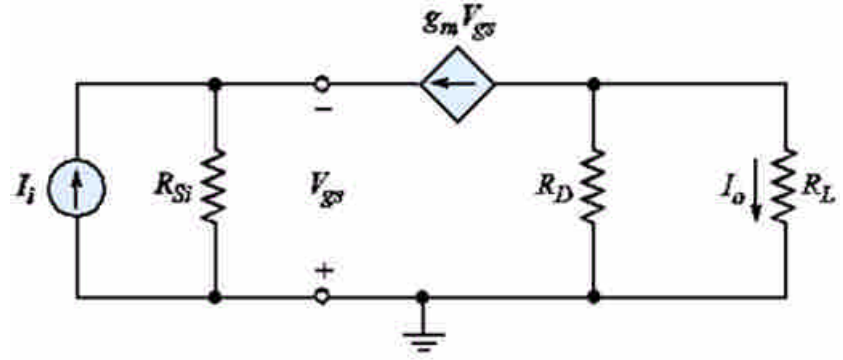
$$V_o = I_i\left(\frac{R_L R_D}{R_D + R_L}\right) \cdot \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right)$$

$$= \left[\frac{(10)(4)}{4 + 10}\right] \cdot \left[\frac{(2)(50)}{1 + (2)(50)}\right] \cdot (0.1) \sin \omega t$$

or

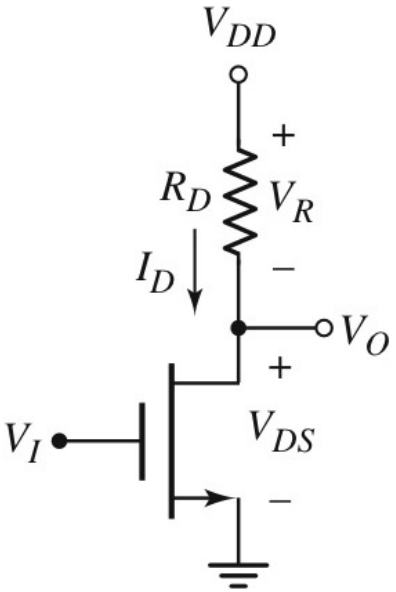
$$V_o = 0.283 \sin \omega t\,\text{V}$$



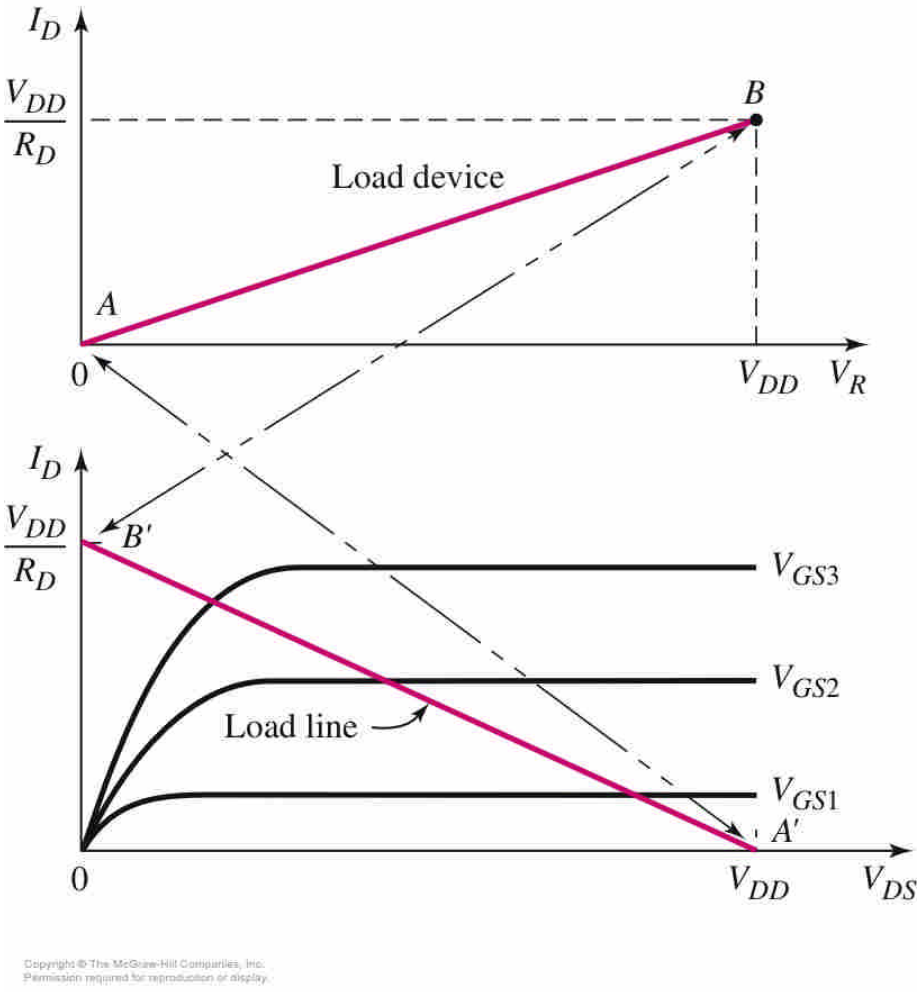



# Load Line

- Load line of a single transistor with a resistive load





# NMOS Amplifiers with Enhancement Load

- An NMOS Enhancement Load Transistor

$$i_D = K_n(v_{DS} - V_{TN})^2$$

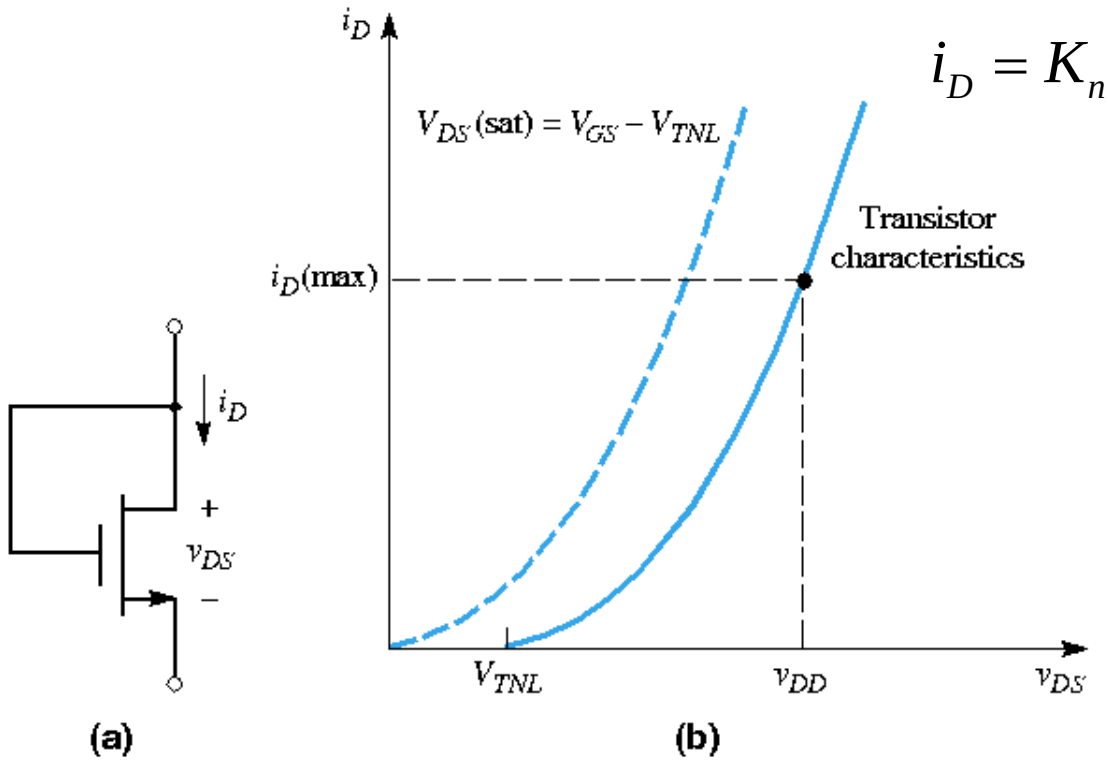



**Figure 6.38** (a) NMOS enhancement-mode transistor with gate and drain connected in a load device configuration and (b) current–voltage characteristics of NMOS enhancement load transistor

# NMOS Amplifiers with Enhancement Load

- An NOMOS Amplifier with Enhancement Load

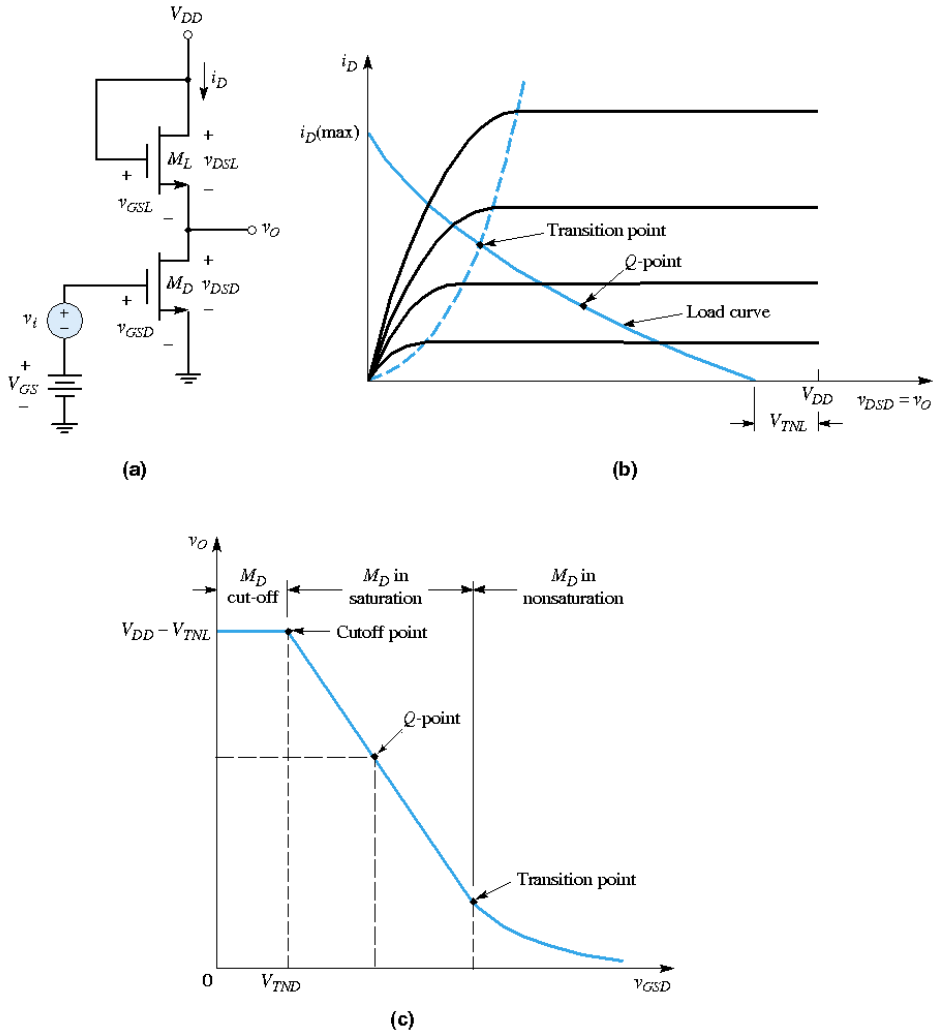



**Figure 6.39** (a) NMOS amplifier with enhancement load device; (b) driver transistor characteristics and enhancement load curve with transition point; and (c) voltage transfer characteristics of NMOS amplifier with enhancement load device

# NMOS Amplifiers with Enhancement Load

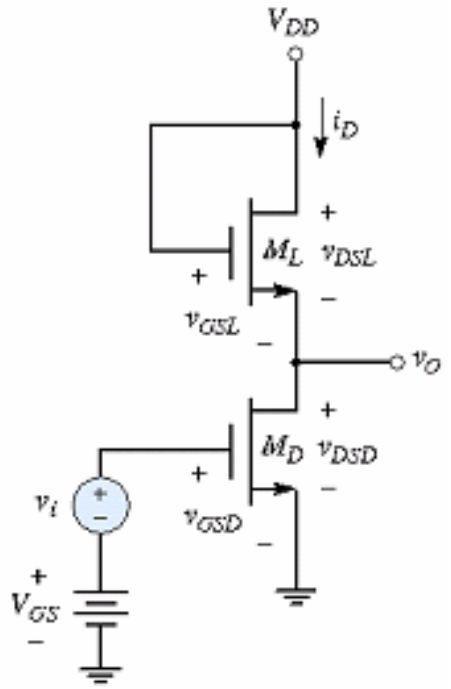
- Small-Signal Voltage Gain

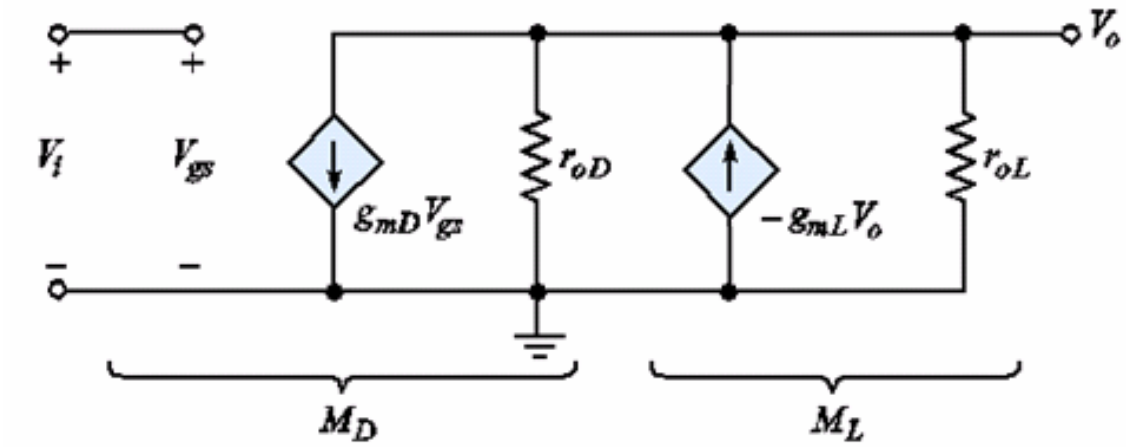
$$g_{mD}V_{gs} + \frac{V_o}{r_{oD} // r_{oL}} = -g_{mL}V_o$$

$$g_{mD}V_{gs} = -\left(\frac{1}{r_{oD} // r_{oL}} + g_{mL}\right)V_o = \frac{-V_o}{r_{oD} // r_{oL} //(1/g_{mL})}$$

$$A_v = -g_{mD}(r_{oD} // r_{oL} //(1/g_{mL}))$$

$$\approx -\frac{g_{mD}}{g_{mL}} = -\sqrt{\frac{K_{nD}}{K_{nL}}} = -\sqrt{\frac{(W/L)_D}{(W/L)_L}}$$



## DESIGN EXAMPLE **4.12**

**Objective:** Design an NMOS amplifier with an enhancement load to meet a set of specifications.

**Specifications:** An NMOS amplifier with the configuration shown in Figure 4.43(a) is to be designed to provide a small-signal voltage gain of $|A_v| = 10$. The $Q$-point is to be in the center of the saturation region. The circuit is to be biased at $V_{DD} = 5$ V.

**Choices:** NMOS transistors with parameters $V_{TN} = 1$ V, $k_n' = 60\ \mu$A/V$^2$, and $\lambda = 0$ are available. The minimum width-to-length ratio is $(W/L)_{\text{min}} = 1$. Tolerances of $\pm 5$ percent in the $k_n'$ and $V_{TN}$ parameters must be considered.

**Solution (ac design):** From Equation (4.50), we have

$$|A_v| = 10 = \sqrt{\frac{(W/L)_D}{(W/L)_L}}$$

which can be written as

$$\left(\frac{W}{L}\right)_D = 100\left(\frac{W}{L}\right)_L$$

If we set $(W/L)_L = 1$, then $(W/L)_D = 100$.

**Solution (dc design):** Setting the currents in the two transistors equal to each oth (both transistors biased in saturation region), we have

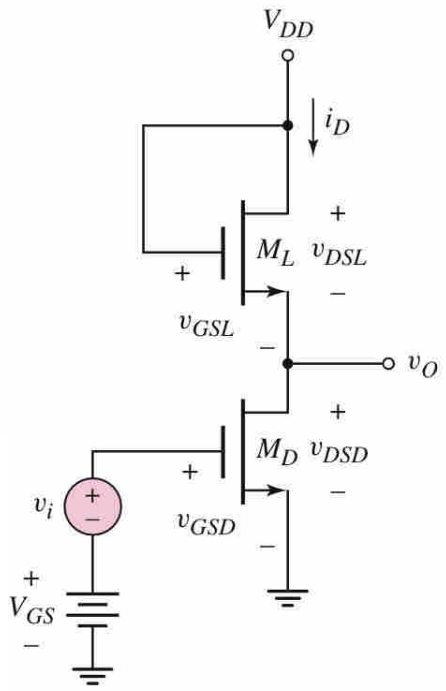
$$i_{DD} = K_{nD}(v_{GSD} - V_{TND})^2 = i_{DL} = K_{nL}(v_{GSL} - V_{TNL})^2$$

From Figure 4.43(a), we see that $v_{GSL} = V_{DD} - v_O$. Substituting, we have

$$K_{nD}(v_{GSD} - V_{TND})^2 = K_{nL}(V_{DD} - v_O - V_{TNL})^2$$

Solving for $v_O$, we have

$$v_O = (V_{DD} - V_{TNL}) - \sqrt{\frac{K_{nD}}{K_{nL}}}(v_{GSD} - V_{TND})$$




(a)

At the transition point,

$$v_{Ot} = v_{DSD}(\text{sat}) = v_{GSDt} - V_{TND}$$

where $v_{GSDt}$ is the gate-to-source voltage of the driver at the transition point. Th

$$v_{GSDt} - V_{TND} = (V_{DD} - V_{TNL}) - \sqrt{\frac{K_{nD}}{K_{nL}}}(v_{GSDt} - V_{TND})$$

Solving for $v_{GSDt}$, we obtain

$$v_{GSDt} = \frac{(V_{DD} - V_{TNL}) + V_{TND}\left(1 + \sqrt{\dfrac{K_{nD}}{K_{nL}}}\right)}{1 + \sqrt{\dfrac{K_{nD}}{K_{nL}}}}$$

Noting that

$$\sqrt{\frac{K_{nD}}{K_{nL}}} = \sqrt{\frac{(W/L)_D}{(W/L)_L}} = 10$$

we find

$$v_{GSDt} = \frac{(5-1) + (1)(1+10)}{1+10} = 1.36\,\text{V}$$

and

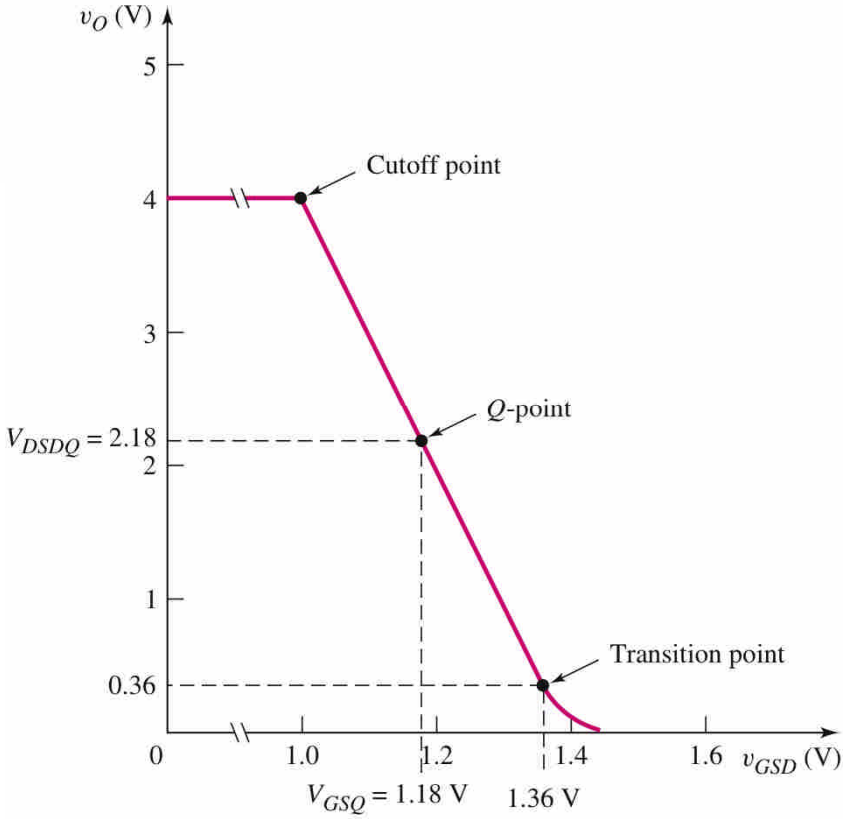
$$v_{Ot} = v_{DSDt} = v_{GSDt} - V_{TND} = 1.36 - 1 = 0.36\,\text{V}$$

Considering the transfer characteristics shown in Figure 4.45, we see that center of the saturation region is halfway between the cutoff point ($v_{GSD}$ $V_{TND} = 1$ V) and the transition point ($v_{GSdt} = 1.36$ V), or

$$V_{GSQ} = \frac{1.36 - 1.0}{2} + 1.0 = 1.18\,\text{V}$$

Also

$$V_{DSDQ} = \frac{4 - 0.36}{2} + 0.36 = 2.18\,\text{V}$$



# NMOS Amplifier with Depletion Load

- An NMOS Depletion Load Transistor

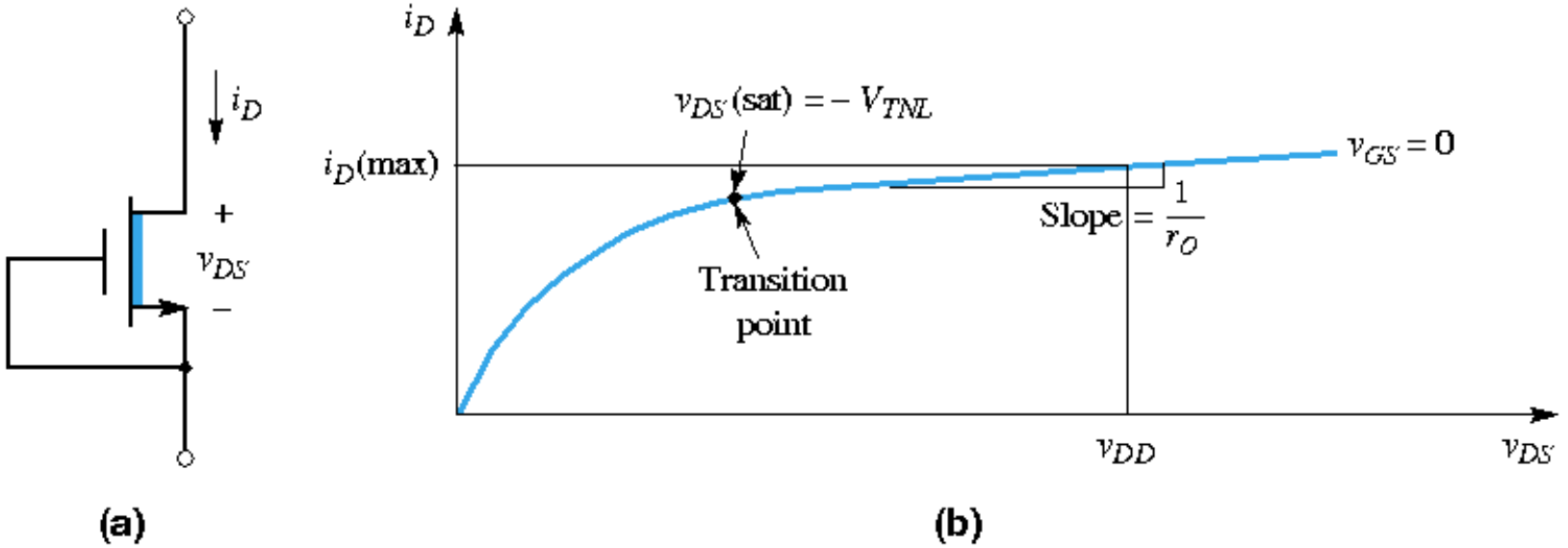



**Figure 6.42** (a) NMOS depletion-mode transistor with gate and source connected in a load device configuration and (b) current–voltage characteristic of NMOS depletion load transistor

# NMOS Amplifier with Depletion Load

- An NMOS Amplifier with Depletion Load

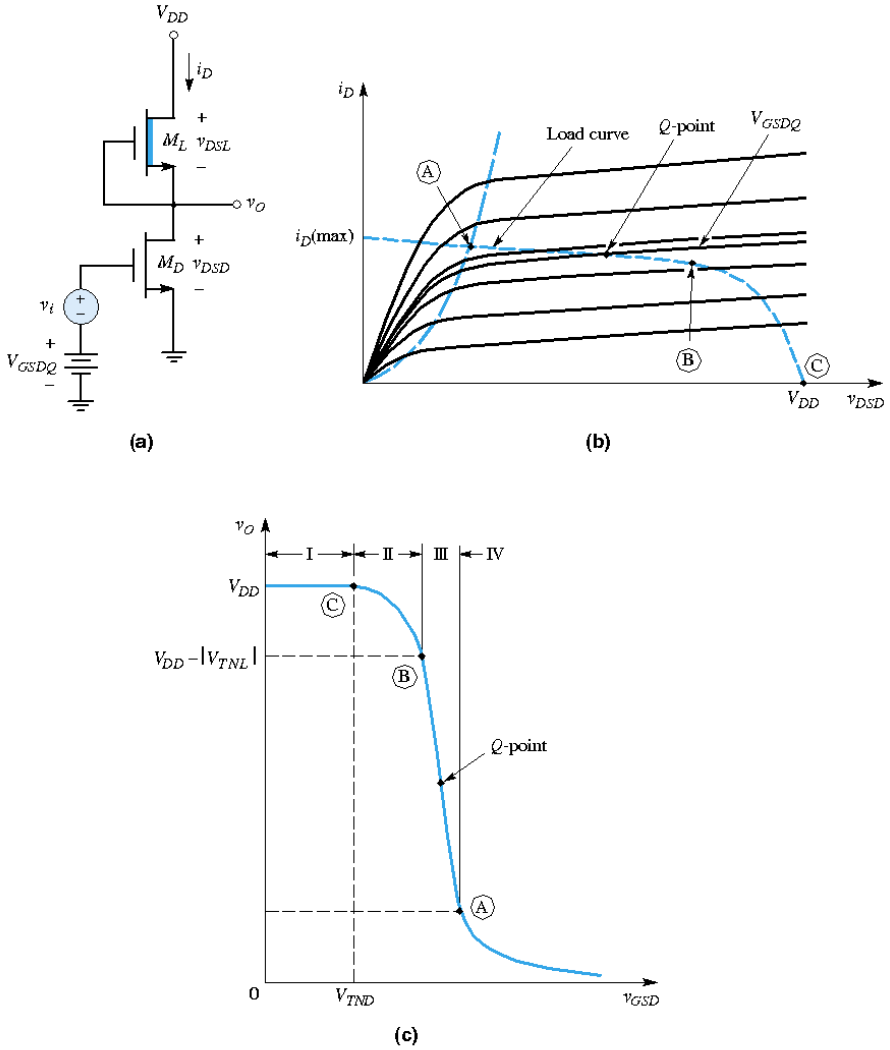
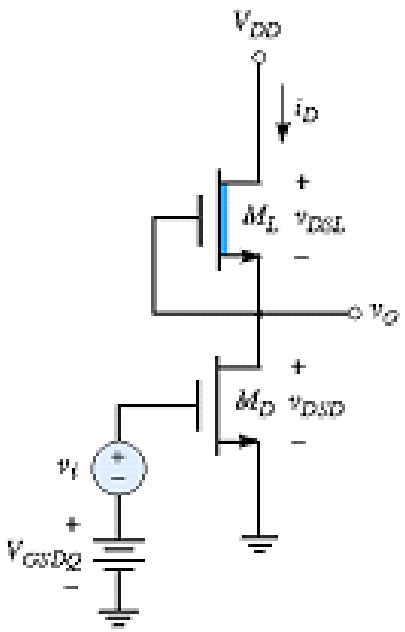



**Figure 6.43** (a) NMOS amplifier with depletion load device; (b) driver transistor characteristics and depletion load curve, with transition points; and (c) voltage transfer characteristics

# NMOS Amplifier with Depletion Load

- Small-Signal Voltage Gain

$$A_v = -g_{mD}(r_{oD} // r_{oL})$$



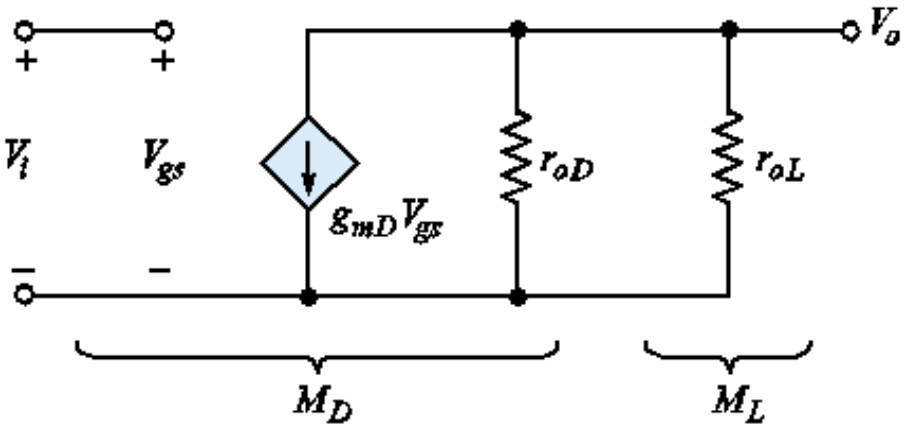




**Figure 6.44** Small-signal equivalent circuit of NMOS inverter with depletion load device

**Example 6.12** **Objective:** Determine the small-signal voltage gain of the NMOS amplifier with depletion load.

For the circuit shown in Figure 6.43(a), assume transistor parameters of $V_{TND} = +0.8\,\text{V}$, $V_{TNL} = -1.5\,\text{V}$, $K_{nD} = 1\,\text{mA/V}^2$, $K_{nL} = 0.2\,\text{mA/V}^2$, and $\lambda_D = \lambda_L = 0.01\,\text{V}^{-1}$. Assume the transistors are biased at $I_{DQ} = 0.2\,\text{mA}$.

**Solution:** The transconductance of the driver is

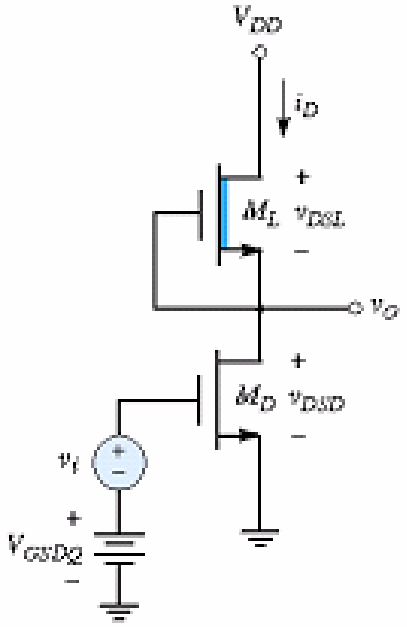
$$g_{mD} = 2\sqrt{K_{nD}I_{DQ}} = 2\sqrt{(1)(0.2)} = 0.894\,\text{mA/V}$$

Since $\lambda_D = \lambda_L$, the output resistances are

$$r_{oD} = r_{oL} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(0.2)} = 500\,\text{k}\Omega$$

The small-signal voltage gain is then

$$A_v = -g_{mD}(r_{oD} \| r_{oL}) = -(0.894)(500 \| 500) = -224$$




**Comment:** The voltage gain of the NMOS amplifier with depletion load is, in general, significantly larger than that with the enhancement load device. The body effect will lower the ideal gain factor.

# NMOS Amplifier with PMOS Load

- Common-Source Amplifier

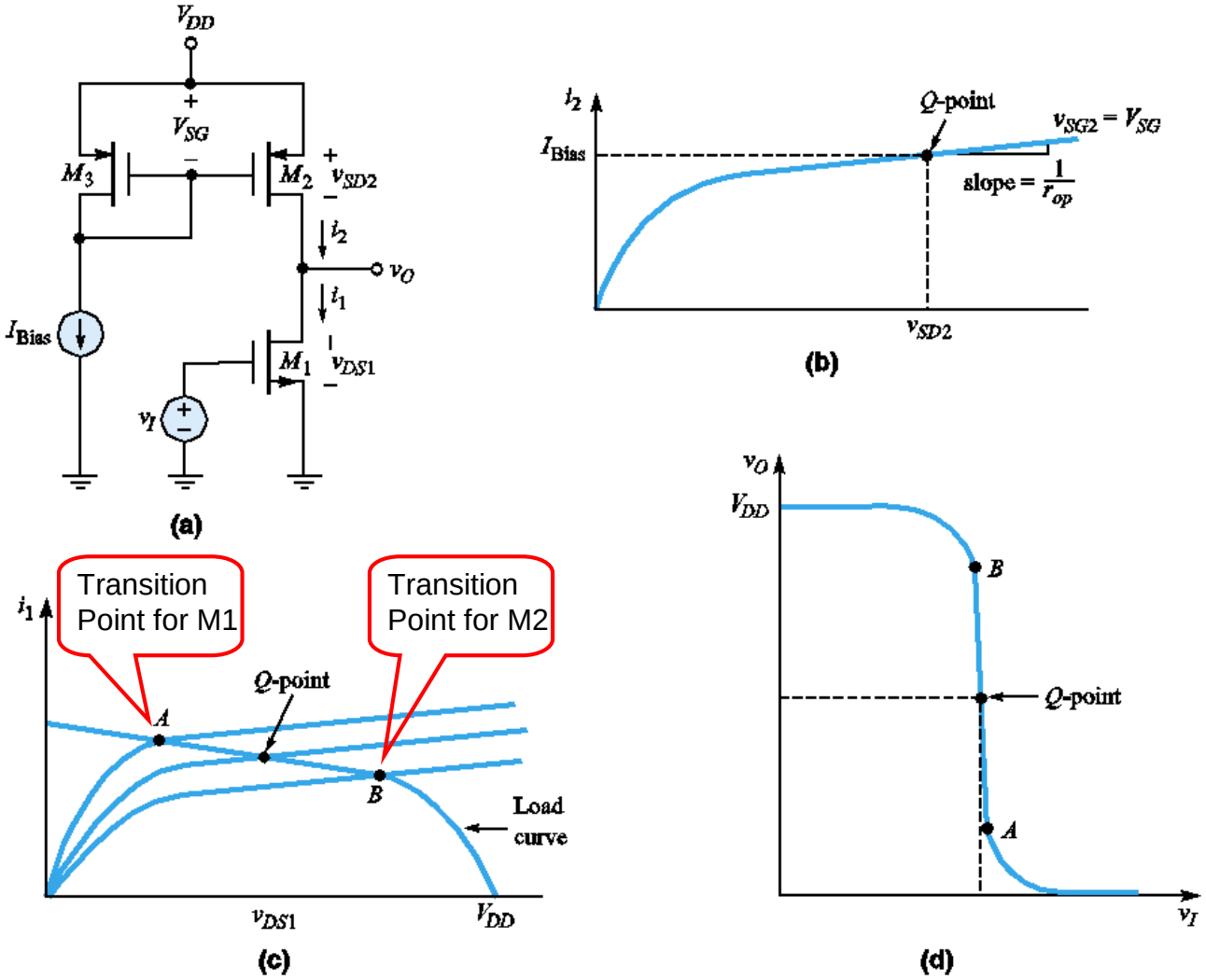
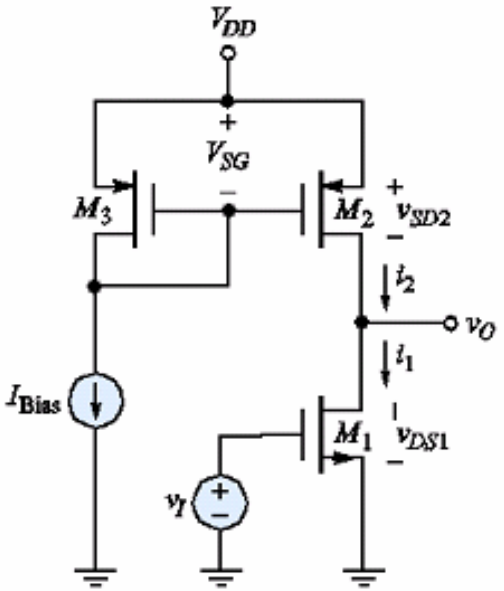



**Figure 6.45** (a) CMOS common-source amplifier; (b) PMOS active load *i–v* characteristic, (c) driver transistor characteristics with load curve, (d) voltage transfer characteristics

# NMOS Amplifier with PMOS Load

- Small-Signal Model for Common-Source Amplifier

$$A_v = -g_{mn}(r_{on} \,//\, r_{op})$$



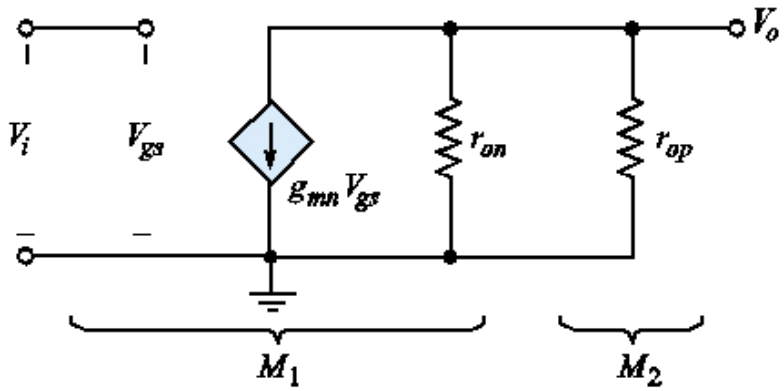




**Figure 6.46** Small-signal equivalent circuit of the CMOS common-source amplifier

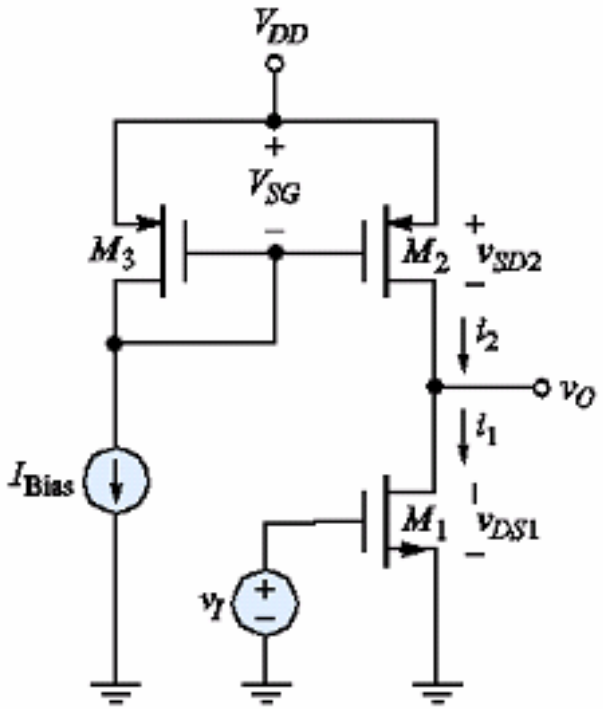
**Example 6.13** **Objective:** Determine the small-signal voltage gain of the CMOS amplifier.

For the circuit shown in Figure 6.45(a), assume transistor parameters of $V_{TN} = +0.8\,\text{V}$, $V_{TP} = -0.8\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $k_p' = 40\,\mu\text{A/V}^2$, $(W/L)_n = 15$, $(W/L)_p = 30$, and $\lambda_n = \lambda_p = 0.01\,\text{V}^{-1}$. Also, assume $I_{\text{Bias}} = 0.2\,\text{mA}$.

**Solution:** The transconductance of the NMOS driver is

$$g_{mn} = 2\sqrt{K_n I_{DQ}} = 2\sqrt{\left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)_n I_{\text{Bias}}}$$

$$= 2\sqrt{\left(\frac{0.08}{2}\right)(15)(0.2)} = 0.693\,\text{mA/V}$$




Since $\lambda_n = \lambda_p$, the output resistances are

$$r_{on} = r_{op} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(0.2)} = 500\,\text{k}\Omega$$

The small-signal voltage gain is then

$$A_v = -g_m(r_{on} \| r_{op}) = -(0.693)(500 \| 500) = -173$$

**Comment:** The voltage gain of the CMOS amplifier is on the same order of magnitude as the NMOS amplifier with depletion load. However, the CMOS amplifier does not suffer from the body effect.

# NMOS Amplifier with PMOS Load

- CMOS Source-Follower and Common-Gate amplifiers

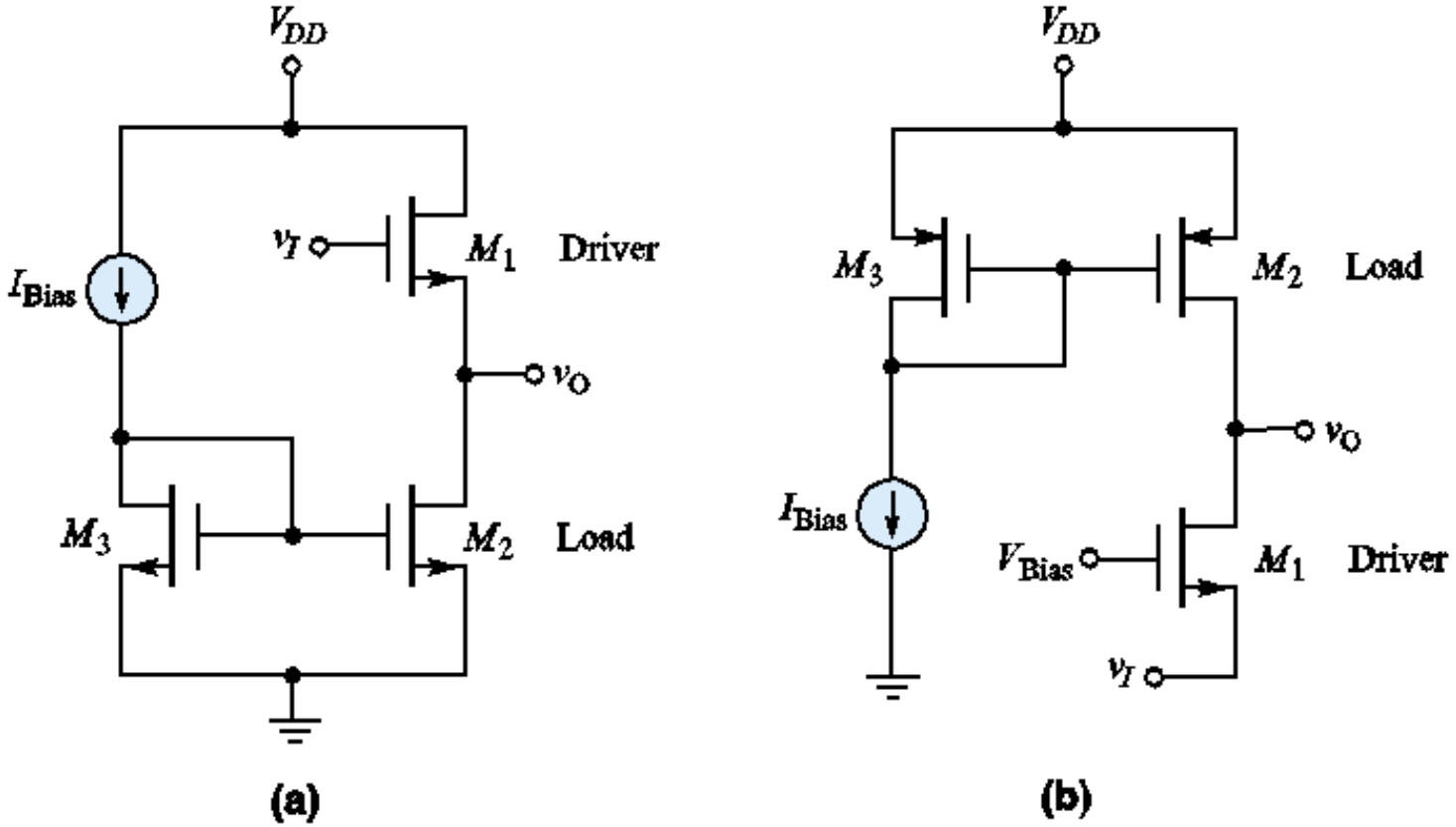



**Figure 6.47** (a) CMOS source-follower amplifier; (b) CMOS common-gate amplifier

## EXAMPLE 4.15

**Objective:** Determine the small-signal voltage gain and output resistance of the source-follower amplifier shown in Figure 4.51(a).

Assume the reference bias current is $I_{\text{Bias}} = 0.20$ mA and the bias voltage is $V_{DD} = 5$ V. Assume that all transistors are matched (identical) with parameters $V_{TN} = 0.8$ V, $K_n = 0.20$ mA/V$^2$, and $\lambda = 0.01$ V$^{-1}$.

We may note that since $M_3$ and $M_2$ are matched transistors and have the same gate-to-source voltages, the drain current in $M_1$ is $I_{D1} = I_{\text{Bias}} = 0.2$ mA.

**Solution (voltage gain):** From Figure 4.51(c), we find the small-signal output age to be

$$V_o = g_{m1} V_{gs} (r_{o1} \| r_{o2})$$

A KVL equation around the outside loop produces

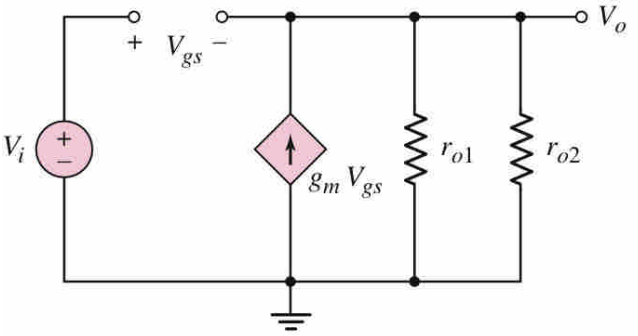
$$V_i = V_{gs} + V_o = V_{gs} + g_{m1} V_{gs} (r_{o1} \| r_{o2})$$

or

$$V_{gs} = \frac{V_i}{1 + g_{m1}(r_{o1} \| r_{o2})}$$

Substituting this equation for $V_{gs}$ into the output voltage expression, we obtain small-signal voltage gain as

$$A_v = \frac{V_o}{V_i} = \frac{g_{m1}(r_{o1} \| r_{o2})}{1 + g_{m1}(r_{o1} \| r_{o2})}$$




The small-signal equivalent circuit parameters are determined to be

$$g_{m1} = 2\sqrt{K_n I_{D1}} = 2\sqrt{(0.20)(0.20)} = 0.40 \text{ mA/V}$$

and

$$r_{o1} = r_{o2} = \frac{1}{\lambda I_D} = \frac{1}{(0.01)(0.20)} = 500 \text{ k}\Omega$$

The small-signal voltage gain is then

$$A_v = \frac{(0.40)(500\|500)}{1 + (0.40)(500\|500)}$$

or

$$A_v = 0.990$$

**Solution (output resistance):** The output resistance can be determined from equivalent circuit shown in Figure 4.51(d). The independent source $V_i$ is set eq zero and a test voltage $V_x$ is applied to the output.

Summing currents at the output node, we find

$$I_x + g_{m1} V_{gs} = \frac{V_x}{r_{o2}} + \frac{V_x}{r_{o1}}$$

From the circuit, we see that $V_{gs} = -V_x$. We then have

$$I_x = V_x \left( g_{m1} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} \right)$$

The output resistance is then given as

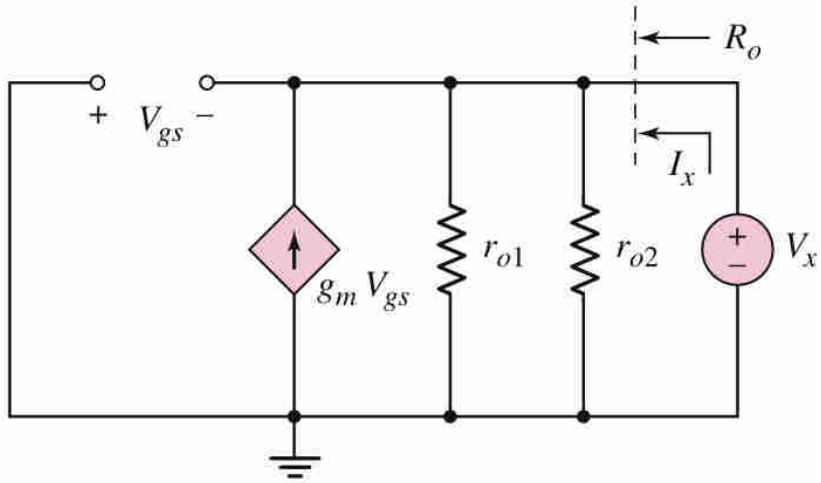
$$R_o = \frac{V_x}{I_x} = \frac{1}{g_{m1}} \| r_{o2} \| r_{o1}$$

We find

$$R_o = \frac{1}{0.40} \| 500 \| 500$$

or

$$R_o = 2.48\,\text{k}\Omega$$



## EXAMPLE 4.16

**Objective:** Determine the small-signal voltage gain and output resistance of common-gate circuit shown in Figure 4.52(a).

Assume the reference bias current is $I_{\text{Bias}} = 0.20$ mA and the bias voltage $V_{DD} = 5$ V. Assume that the transistor parameters are $V_{TN} = +0.80$ V, $V_{TP}$ $-0.80$ V, $K_n = 0.20$ mA/V$^2$, $K_p = 0.20$ mA/V$^2$, and $\lambda_n = \lambda_p = 0.01\,\text{V}^{-1}$.

We may note that, since $M_2$ and $M_3$ are matched transistors and have the s source-to-gate voltage, the bias current in $M_1$ is $I_{D1} = I_{\text{Bias}} = 0.20$ mA.

**Solution (voltage gain):** From Figure 4.52(b), we can sum currents at the out node and obtain

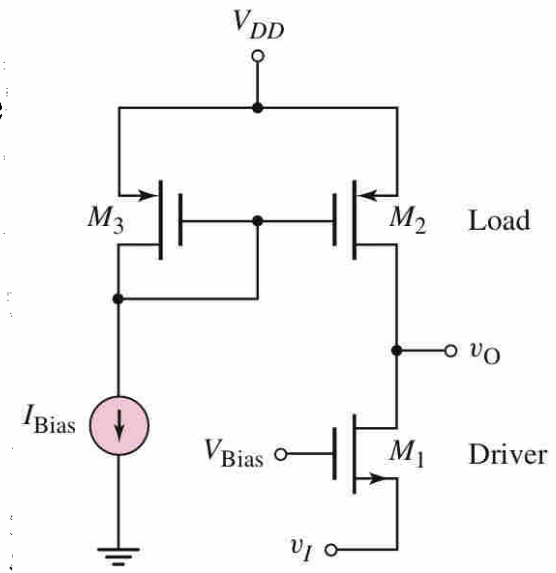
$$\frac{V_o}{r_{o2}} + g_{m1}V_{gs} + \frac{V_o - (-V_{gs})}{r_{o1}} = 0$$

or

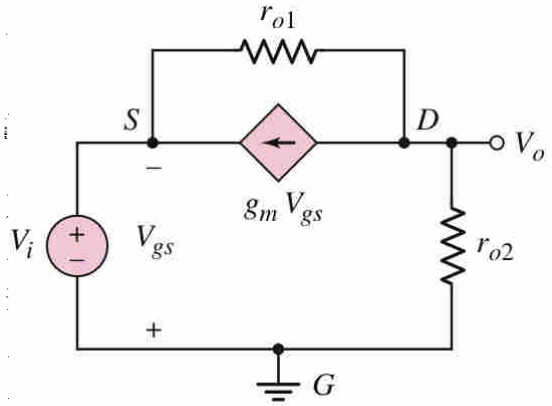
$$V_o\left(\frac{1}{r_{o2}} + \frac{1}{r_{o1}}\right) + V_{gs}\left(g_{m1} + \frac{1}{r_{o1}}\right) = 0$$

From the circuit, we see that $V_{gs} = -V_i$. We then find the small-signal voltage g to be

$$A_v = \frac{\left(g_{m1} + \dfrac{1}{r_{o1}}\right)}{\left(\dfrac{1}{r_{o2}} + \dfrac{1}{r_{o1}}\right)}$$




(a)




(b)

We find the small-signal equivalent circuit parameters to be

$$g_{m1} = 2\sqrt{K_n I_{D1}} = 2\sqrt{(0.20)(0.20)} = 0.40 \text{ mA/V}$$

and

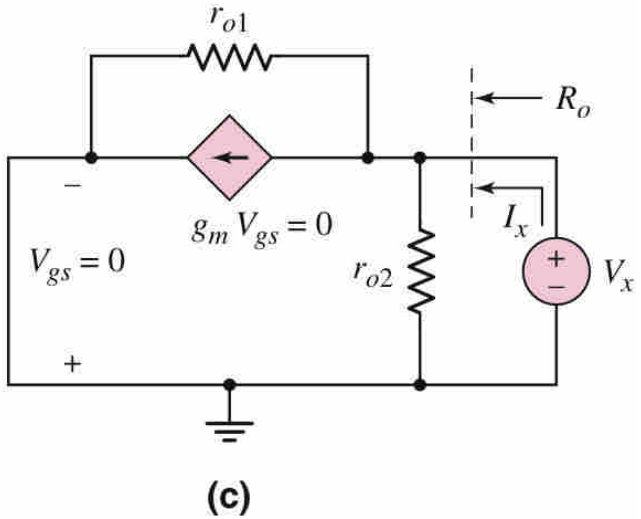
$$r_{o1} = r_{o2} = \frac{1}{\lambda I_{D1}} = \frac{1}{(0.01)(0.20)} = 500\,\text{k}\Omega$$

We then find

$$A_v = \frac{\left(0.40 + \frac{1}{500}\right)}{\left(\frac{1}{500} + \frac{1}{500}\right)}$$

or

$$A_v = 101$$




**Solution (output resistance):** The output resistance can be found from Figure 4.52( Summing currents at the output node, we find

$$I_x = \frac{V_x}{r_{o2}} + g_{m1} V_{gs} + \frac{V_x - (-V_{gs})}{r_{o1}}$$

However, $V_{gs} = 0$ so that $g_{m1} V_{gs} = 0$. We then find

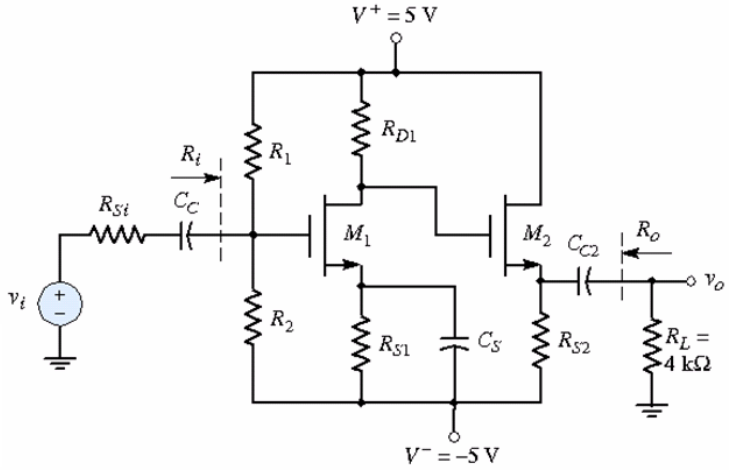
$$R_o = \frac{V_x}{I_x} = r_{o1} \| r_{o2} = 500 \| 500$$

or

$$R_o = 250\,\text{k}\Omega$$

**Example 6.16** **Objective:** Determine the small-signal voltage gain of a multistage cascade circuit.

Consider the circuit shown in Figure 6.49 with transistor and circuit parameters given in Example 6.14.




**Solution:** The small-signal transconductance parameters are

$$g_{m1} = 2K_{n1}(V_{GS1} - V_{TN1}) = 2(0.50)(1.83 - 1.2) = 0.63\,\text{mA/V}$$

and

$$g_{m2} = 2K_{n2}(V_{GS2} - V_{TN2}) = 2(0.2)(2.78 - 1.2) = 0.632\,\text{mA/V}$$

The small-signal equivalent circuit is shown in Figure 6.51.

The output voltage is

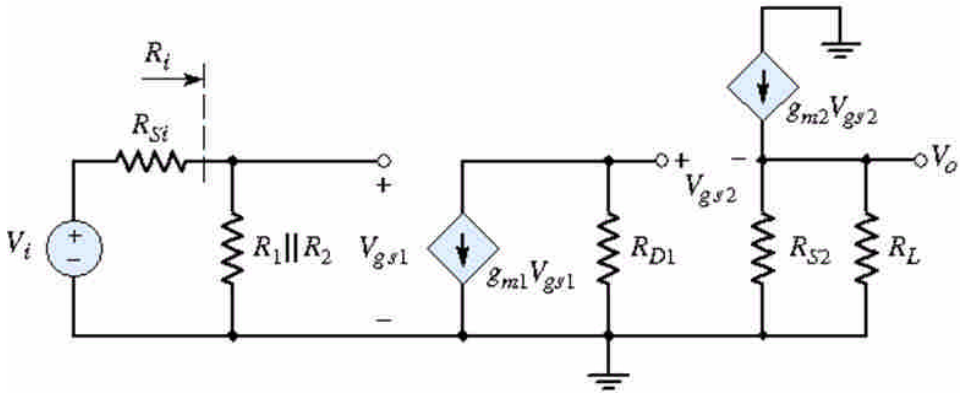
$$V_o = g_{m2}V_{gs2}(R_{S2} \| R_L)$$

Also,

$$V_{gs2} + V_o = -g_{m1}V_{gs1}R_{D1}$$

where

$$V_{gs1} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i$$




Then

$$V_{gs2} = -g_{m1}R_{D1}\left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i - V_o$$

Therefore

$$V_o = g_{m2}\left[-g_{m1}R_{D1}\left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i - V_o\right](R_{S2} \| R_L)$$

The small-signal voltage gain is then

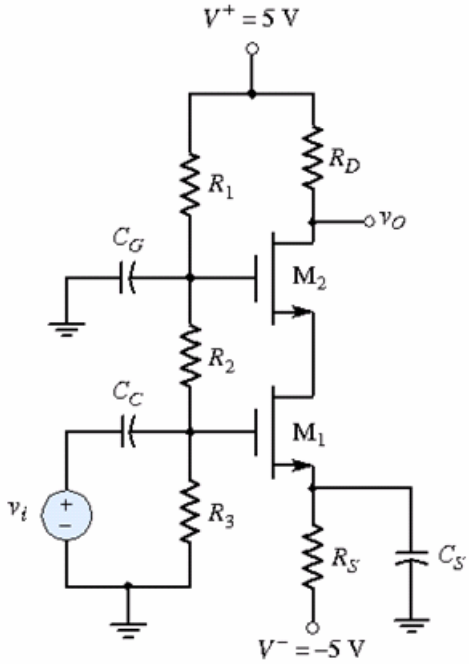
$$A_v = \frac{V_o}{V_i} = \frac{-g_{m1}g_{m2}R_{D1}(R_{S2} \| R_L)}{1 + g_{m2}(R_{S2} \| R_L)} \cdot \left(\frac{R_i}{R_i + R_{Si}}\right)$$

or

$$A_v = \frac{-(0.63)(0.632)(16.1)(8 \| 4)}{1 + (0.632)(8 \| 4)} \cdot \left(\frac{100}{100 + 4}\right) = -6.13$$

**Example 6.17** **Objective:** Determine the small-signal voltage gain of a cascode circuit.

For the circuit shown in Figure 6.50, the transistor and circuit parameters are as given in Example 6.15. The input signal to the circuit is an ideal voltage source.




**Solution:** Since the transistors are identical, the small-signal transconductance parameters of the two transistors are equal. Therefore,

$$g_{m1} = g_{m2} = 2K_n(V_{GS} - V_{TN}) = 2(0.8)(1.91 - 1.2) = 1.14\,\text{mA/V}$$

The small-signal equivalent circuit is shown in Figure 6.52. Transistor $M_1$ supplies the source current of $M_2$ with the signal current $(g_{m1}V_i)$. Transistor $M_2$ acts as a current follower and passes this current on to its drain terminal. The output voltage is therefore

$$V_o = -g_{m1}V_{gs1}R_D$$

Since $V_{gs1} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_{m1}R_D$$

or

$$A_v = -(1.14)(2.5) = -2.85$$

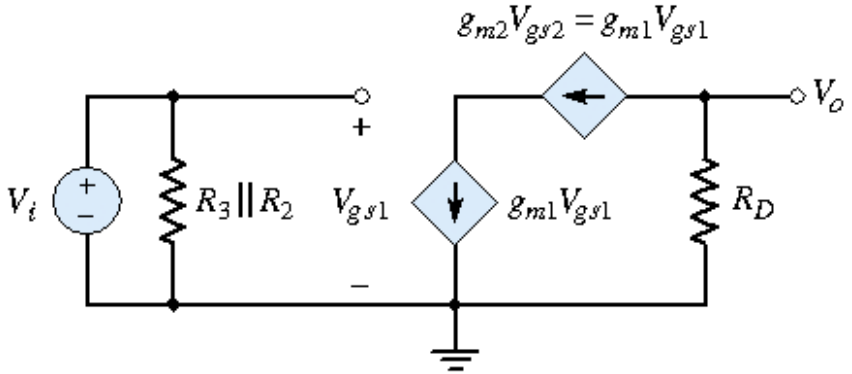



**Figure 6.52** Small-signal equivalent circuit of NMOS cascode circuit

# Basic JFET Amplifiers

- Transconductance in the Small-Signal Equivalent Circuit

$$v_{GS} = V_{GS} + v_i = V_{GS} + v_{gs}$$

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left[\left(1 - \frac{V_{GS}}{V_P}\right) - \left(\frac{v_{gs}}{V_P}\right)\right]^2$$

$$= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 - 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\left(\frac{v_{gs}}{V_P}\right) + I_{DSS}\left(\frac{v_{gs}}{V_P}\right)^2$$

$$= I_{DQ} + i_d$$

$$i_d = \frac{2I_{DSS}}{(-V_p)}\left(1 - \frac{V_{GS}}{V_P}\right)v_{gs} = g_m v_{gs}$$

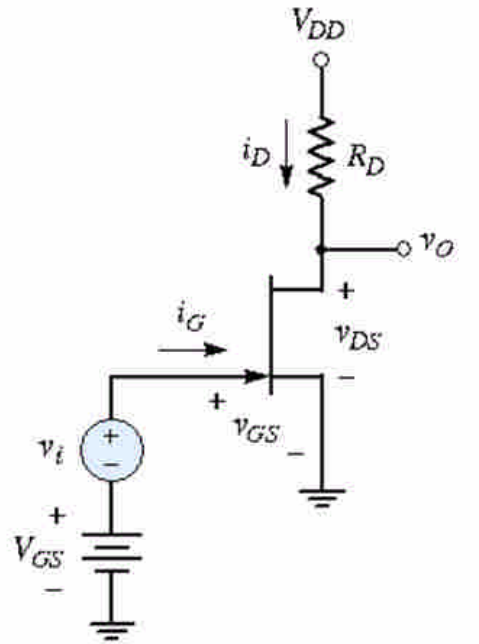



**Figure 6.53** JFET common-source circuit with time-varying signal source in series with gate dc source

- Since $V_P$ is negative for n-channel JFETs, the transconductance $g_m$ is positive. A relationship that applies to both n-channel and p-channel JFETs is

$$g_m = \frac{2I_{DSS}}{|V_p|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

# Basic JFET Amplifiers

- Finite Output Resistance

$$i_D = I_{DSS}\left(1-\frac{v_{GS}}{V_P}\right)^2(1+\lambda v_{DS})$$

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}}$$

$$= \left[\lambda I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2\right]^{-1}$$

$$\approx [\lambda I_{DQ}]^{-1}$$

- Small-Signal Model

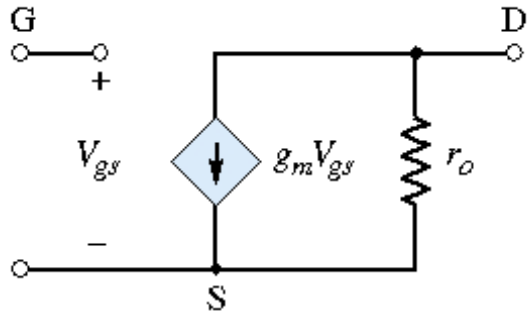



**Figure 6.54** Small-signal equivalent circuit of n-channel JFET

**Example 6.18** **Objective:** Determine the small-signal voltage gain of a JFET amplifier.

Consider the circuit shown in Figure 6.55 with transistor parameters $I_{DSS} = 12\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0.008\,\text{V}^{-1}$. Determine the small-signal voltage gain $A_v = v_o/v_i$.

**Solution:** The dc quiescent gate-to-source voltage is determined from

$$V_{GSQ} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} - I_{DQ}R_S$$

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2$$

Combining these two equations produces

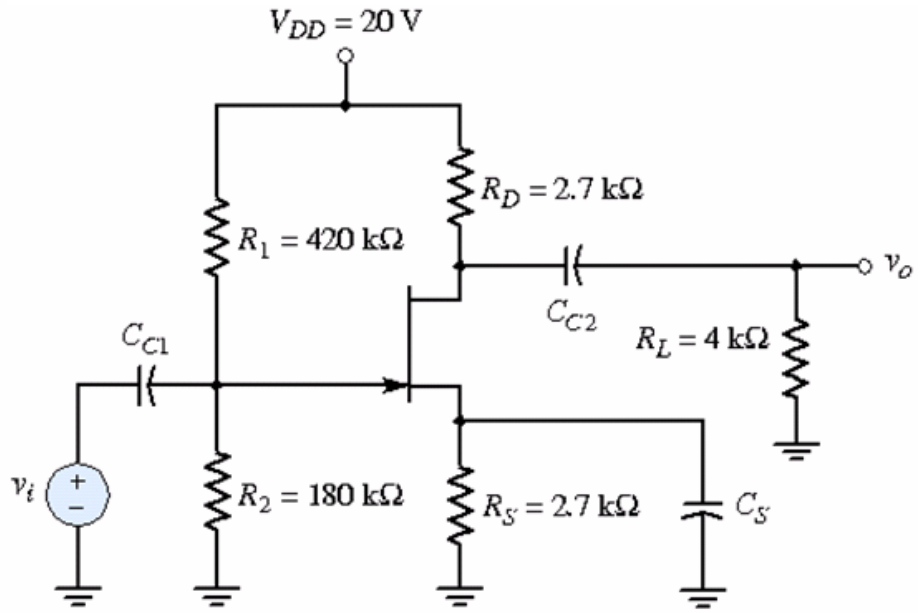
$$V_{GSQ} = \left(\frac{180}{180 + 420}\right)(20) - (12)(2.7)\left(1 - \frac{V_{GSQ}}{(-4)}\right)^2$$

which reduces to

$$2.025V_{GSQ}^2 + 17.2V_{GSQ} + 26.4 = 0$$

The appropriate solution is

$$V_{GSQ} = -2.01\,\text{V}$$



The quiescent drain current is

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 = (12)\left(1 - \frac{(-2.01)}{(-4)}\right)^2 = 2.97\,\text{mA}$$

The small-signal parameters are then

$$g_m = \frac{2I_{DSS}}{(-V_P)}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2(12)}{(4)}\left(1 - \frac{(-2.01)}{(-4)}\right) = 2.98\,\text{mA/V}$$

and

$$r_o = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.008)(2.97)} = 42.1\,\text{k}\Omega$$

The small-signal equivalent circuit is shown in Figure 6.56.

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D \| R_L)$$

or

$$A_v = -(2.98)(42.1 \| 2.7 \| 4) = -4.62$$

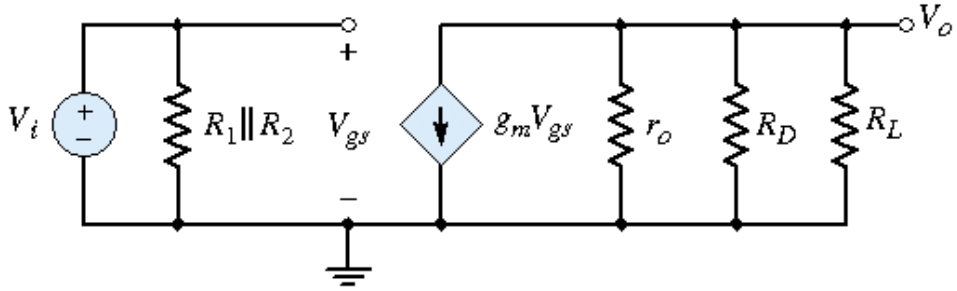



**Figure 6.56** Small-signal equivalent circuit of common-source JFET, assuming bypass capacitor acts as a short circuit

**Design Example 6.19** **Objective:** Design a JFET source-follower circuit with a specified small-signal voltage gain.

For the source-follower circuit shown in Figure 6.57, the transistor parameters are: $I_{DSS} = 12\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0.01\,\text{V}^{-1}$. Determine $R_S$ and $I_{DQ}$ such that the small-signal voltage gain is at least $A_v = v_o/v_i = 0.90$.

**Solution:** The small-signal equivalent circuit is shown in Figure 6.58. The output voltage is

$$V_o = g_m V_{gs}(R_S \| R_L \| r_o)$$

Also

$$V_i = V_{gs} + V_o$$

or

$$V_{gs} = V_i - V_o$$

Therefore, the output voltage is

$$V_o = g_m(V_i - V_o)(R_S \| R_L \| r_o)$$

The small-signal voltage gain becomes

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_S \| R_L \| r_o)}{1 + g_m(R_S \| R_L \| r_o)}$$

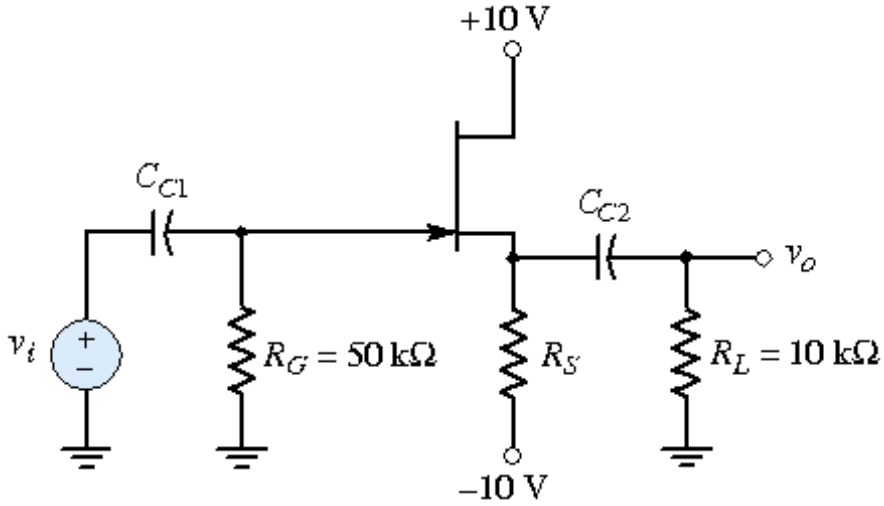



**Figure 6.57** JFET source-follower circuit

As a first approximation, assume $r_o$ is sufficiently large for the effect of $r_o$ to be neglected.

The transconductance is

$$g_m = \frac{2I_{DSS}}{(-V_P)}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2(12)}{4}\left(1 - \frac{V_{GS}}{(-4)}\right)$$

If we pick a nominal transconductance value of $g_m = 2\,\text{mA/V}$, then $V_{GS} = -2.67\,\text{V}$ and the quiescent drain current is

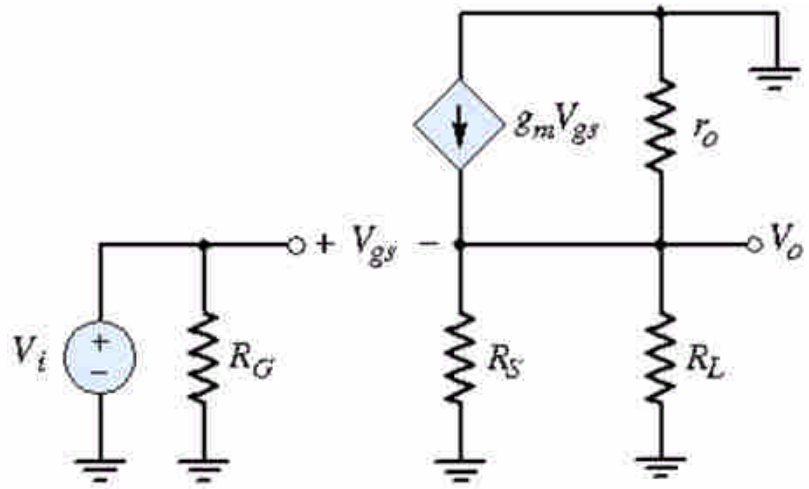
$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = (12)\left(1 - \frac{(-2.67)}{(-4)}\right)^2 = 1.33\,\text{mA}$$

The value of $R_S$ is then determined from

$$R_S = \frac{-V_{GS} - (-10)}{I_{DQ}} = \frac{2.67 + 10}{1.33} = 9.53\,\text{k}\Omega$$

Also, the value of $r_o$ is

$$r_o = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(1.33)} = 75.2\,\text{k}\Omega$$




The small-signal voltage gain, including the effect of $r_o$, is

$$A_v = \frac{g_m(R_S \| R_L \| r_o)}{1 + g_m(R_S \| R_L \| r_o)} = \frac{(2)(9.53 \| 10 \| 75.2)}{1 + (2)(9.53 \| 10 \| 75.2)} = 0.902$$