The Bipolar Junction Transistor (BJT)

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Bipolar Transistor Structures

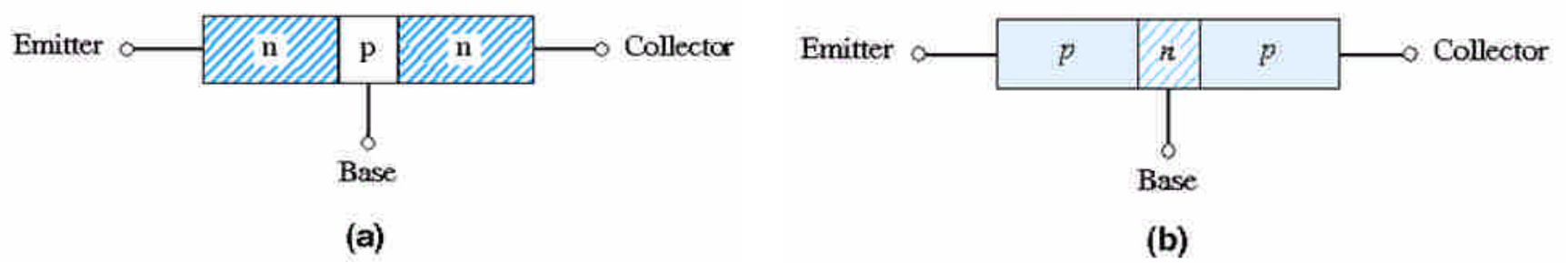


Figure 3.1 Simple geometry of bipolar transistors: (a) npn and (b) pnp

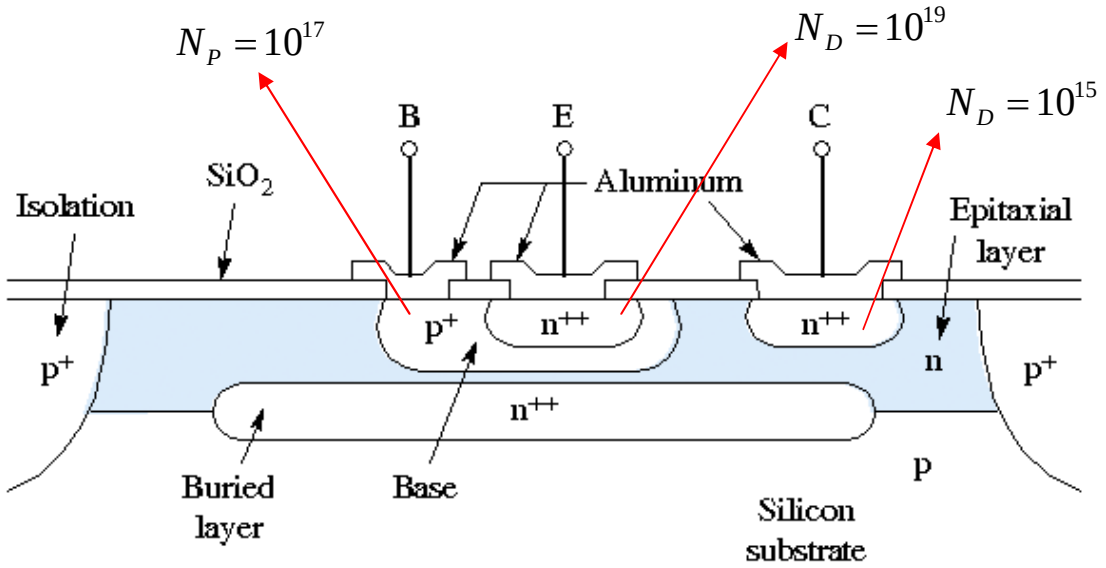


Figure 3.2 Cross section of a conventional integrated circuit npn bipolar transistor

Forward-Active Mode in the NPN Transistor

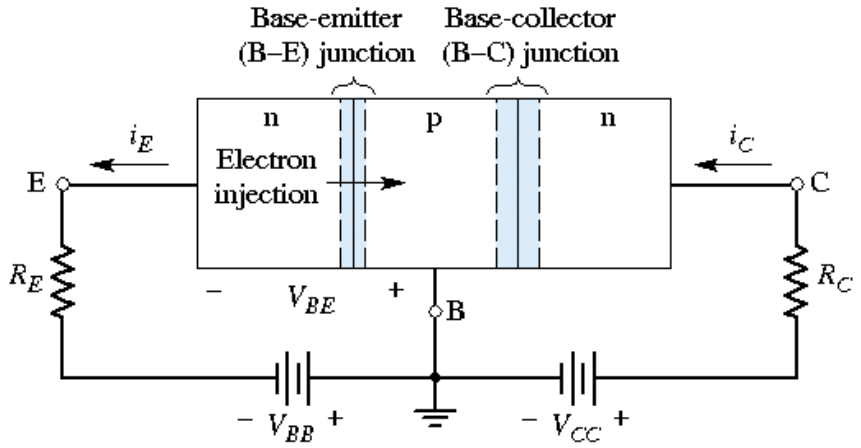
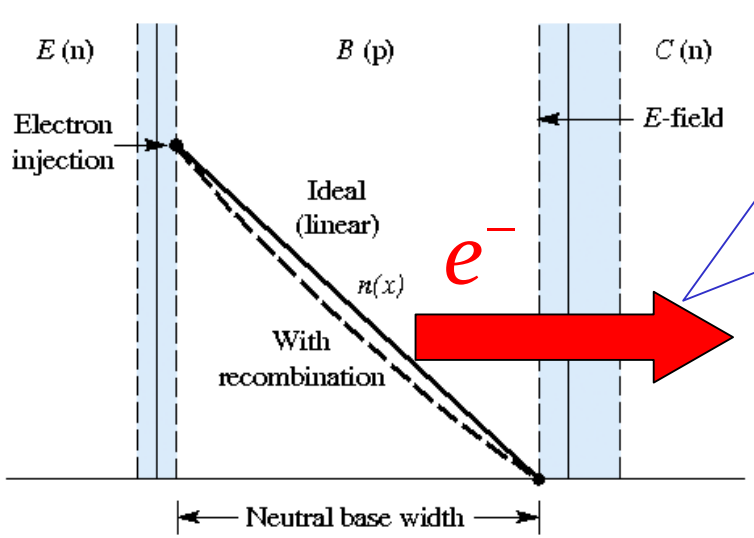


Figure 3.3 An npn bipolar transistor biased in the forward-active mode



Because of the large concentration gradient in the base region, electrons injected from the emitter diffuse across the base into the BC space-charge region, where the E-field sweeps them into the collector region.

Figure 3.4 Minority carrier electron concentration across the base region of an npn bipolar transistor biased in the forward-active mode

Currents in Emitter, Collector, and Base

- Emitter Current: Exponential function of the BE voltage
- Collector Current: Ignoring the recombination in the base region (the base width is very tiny, micrometer), the collect current is proportional to the emitter injection current and is independent of the reverse-biased BC voltage. Hence, the collector current is controlled by the BE voltage.
- Base Current:
  - ✓ BE forward-biased current i_{B1}
  - ✓ Base recombination current i_{B2}

$$\because N_{D,E} >> N_{P,B}$$

$$\therefore i_C >> i_{B1},$$

$$i_E = i_B + i_C \approx i_{B1} + i_C$$

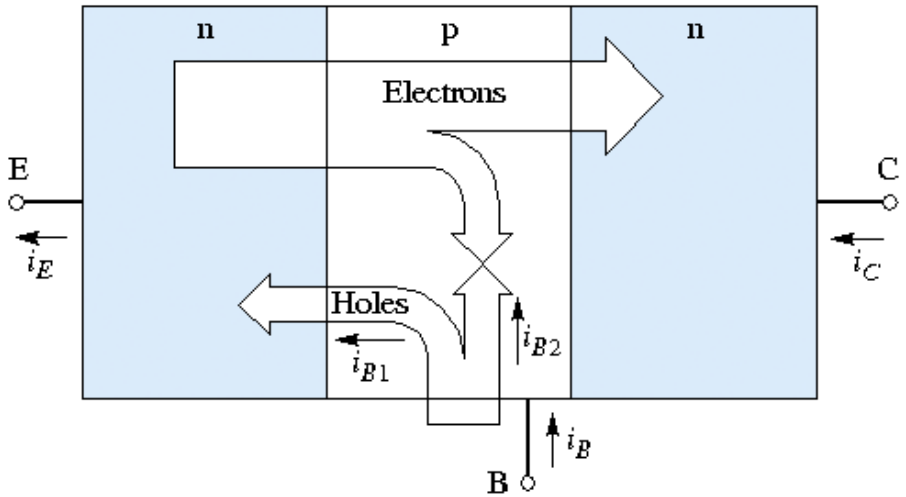


Figure 3.5 Electron and hole currents in an npn transistor biased in the forward-active mode

Common-Emitter Configuration

$$\frac{i_C}{i_B} = \beta$$ Common-emitter current gain

$$i_E = i_B + i_C = (1+\beta)i_B$$

$$i_C = \frac{\beta}{(1+\beta)} i_E$$

The power supply voltage Vcc must be sufficiently large to keep BC junction reverse biased.

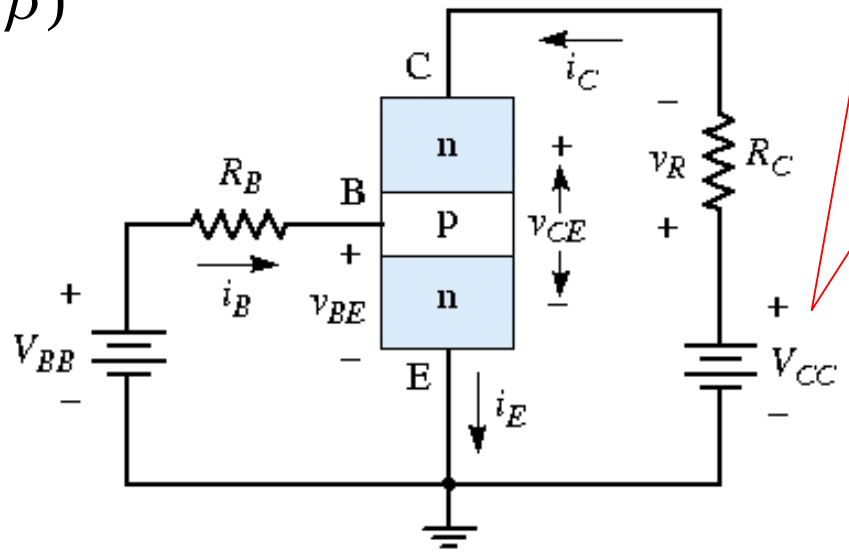


Figure 3.6 An npn transistor circuit in the common-emitter configuration

Example 3.1 **Objective:** Calculate the collector and emitter currents, given the base current and current gain.

Assume a common-emitter current gain of $\beta = 150$ and a base current of $i_B = 15\,\mu\text{A}$. Also assume that the transistor is biased in the forward-active mode.

Solution: The relation between collector and base currents gives

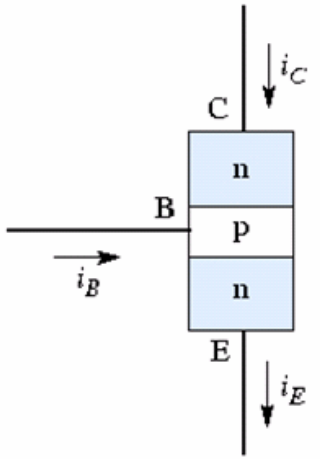
$$i_C = \beta i_B = (150)(15\,\mu\text{A}) \Rightarrow 2.25\,\text{mA}$$

and the relation between emitter and base currents yields

$$i_E = (1 + \beta)i_B = (151)(15\,\mu\text{A}) \Rightarrow 2.27\,\text{mA}$$

From Equation (3.11), the common-base current gain is

$$\alpha = \frac{\beta}{1 + \beta} = \frac{150}{151} = 0.9934$$



Comment: For reasonable values of β, the collector and emitter currents are nearly equal, and the common-base current gain is nearly 1.

Forward-Active Mode in the PNP Transistor

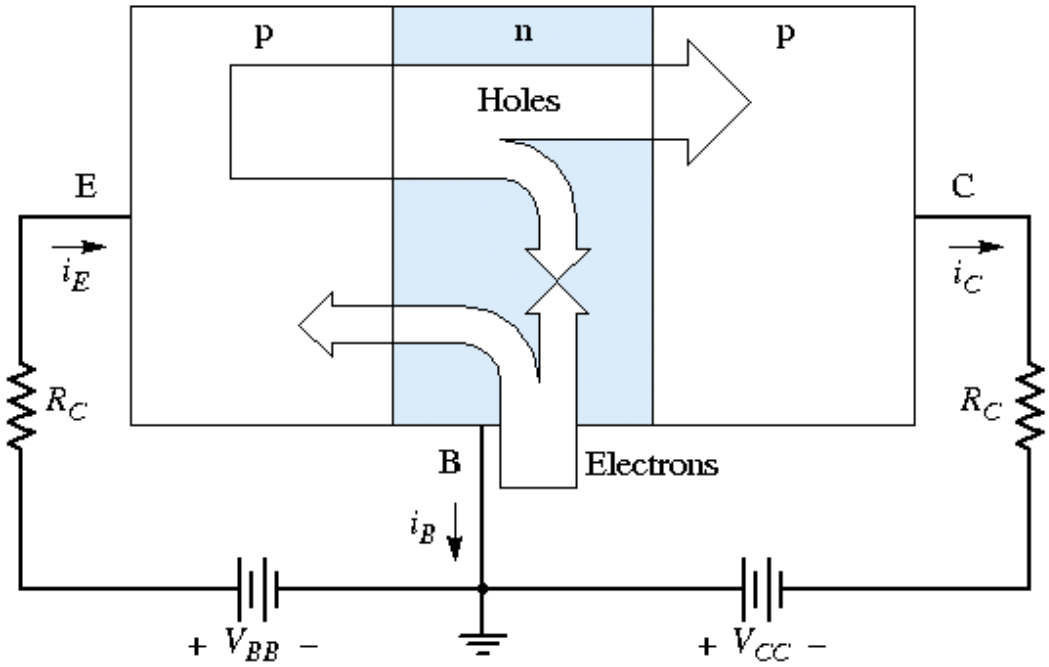


Figure 3.7 Electron and hole currents in a pnp transistor biased in the forward-active mode

Circuit Symbols and Conventions

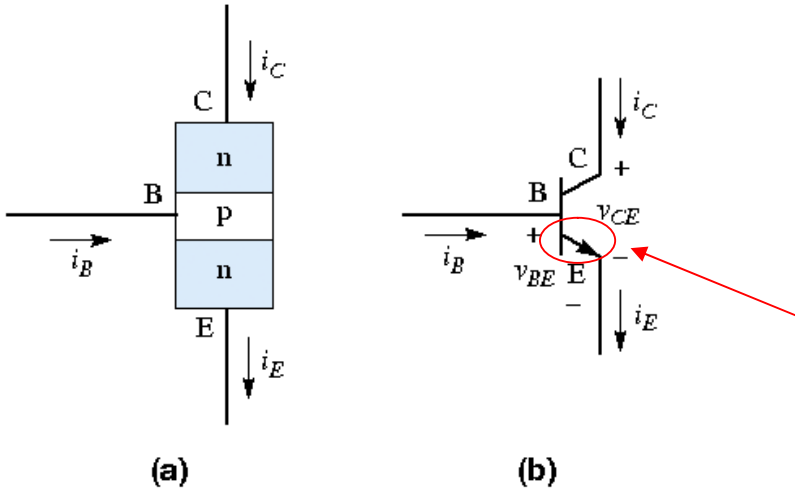


Figure 3.8 npn bipolar transistor: (a) simple block diagram and (b) circuit symbol

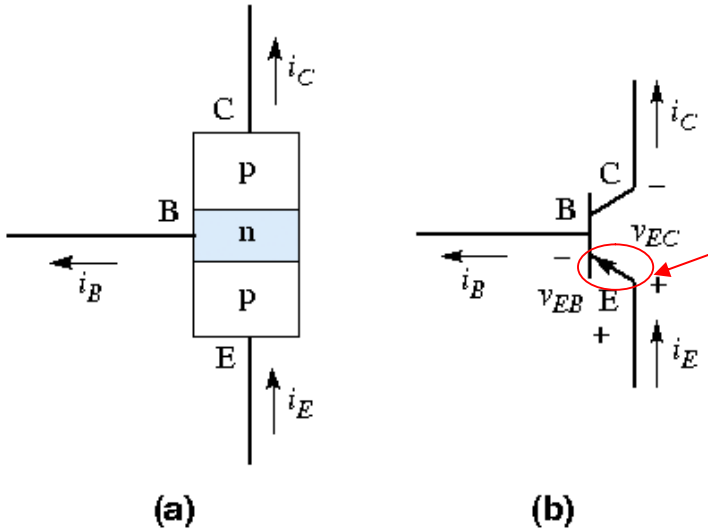


Figure 3.9 pnp bipolar transistor: (a) simple block diagram and (b) circuit symbol

The arrowhead is always placed on the emitter terminal, and it indicates the direction of the emitter current.

Common-Emitter Circuits

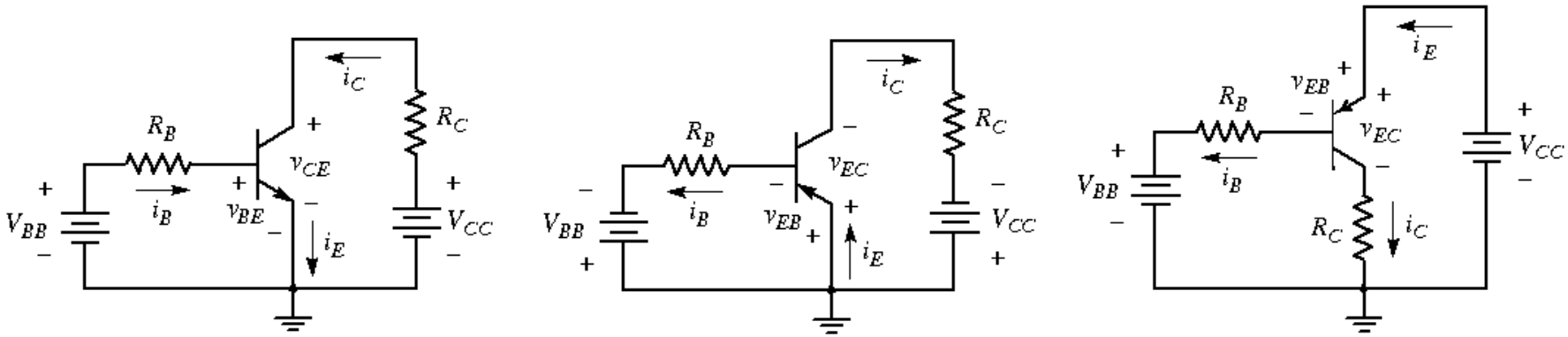


Figure 3.10 Common-emitter circuits: (a) with an npn transistor, (b) with a pnp transistor, and (c) with a pnp transistor biased with a positive voltage source

Table 3.1 Summary of the bipolar current–voltage relationships in the active region

npn	pnp
$i_E = I_S e^{v_{BE}/V_T}$	$i_E = I_S e^{v_{EB}/V_T}$
$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{BE}/V_T}$	$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{EB}/V_T}$
$i_B = \dfrac{i_C}{\beta_F} = \dfrac{\alpha_F I_S}{\beta_F} e^{v_{BE}/V_T}$	$i_B = \dfrac{i_C}{\beta_F} = \dfrac{\alpha_F I_S}{\beta_F} e^{v_{EB}/V_T}$
For both transistors	
$i_C = \beta_F i_B$	$\alpha_F = \dfrac{\beta_F}{1+\beta_F}$
$i_E = (1+\beta_F) i_B$	$\beta_F = \dfrac{\alpha_F}{1-\alpha_F}$
$i_C = \left(\dfrac{\beta_F}{1+\beta_F}\right) i_E = \alpha_F i_E$	

Current-Voltage Characteristics for CB Voltage

- The collector current is nearly independent of the CB voltage as long as the BC junction is reverse biased.

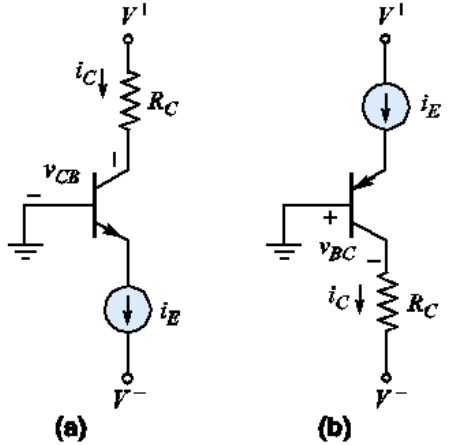


Figure 3.11 Common-base circuit configurations: (a) an npn transistor and (b) a pnp transistor

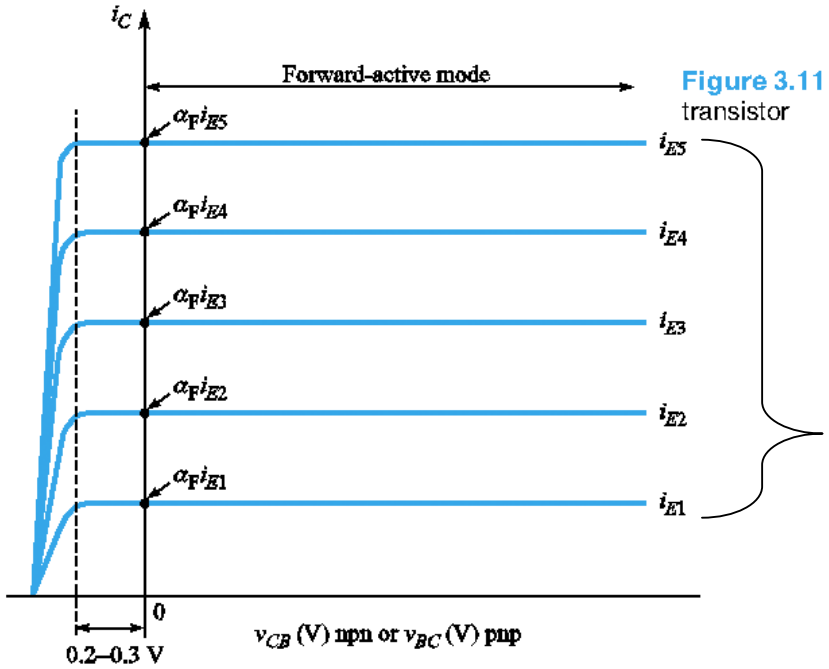


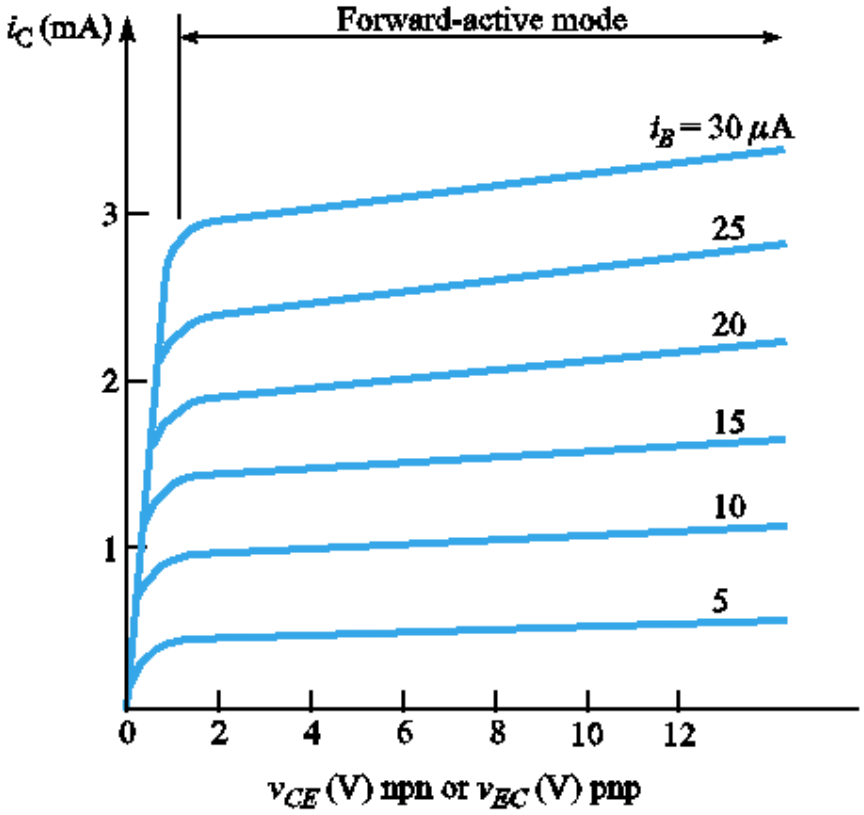
Figure 3.12 Transistor current–voltage characteristics of the common-base circuit

$$\alpha_F = \frac{i_C}{i_E} = \frac{\beta}{1+\beta} \approx 1$$

Emitter is like a constant-current source.

Current-Voltage Characteristics for CE Voltage

- For forward-active mode, the BC junction must be reverse biased, which means that Vce must be greater than approximately Vbe(on). There is a finite to the curves.



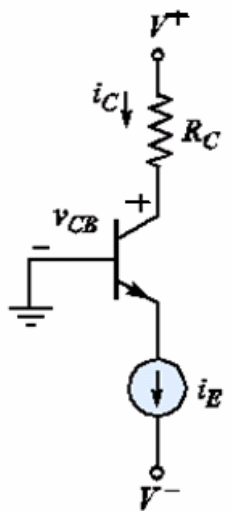


Figure 3.13 Transistor current–voltage characteristics of the common-emitter circuit

Early Voltage

- When the current-voltage characteristic curves are extrapolated to zero current, they meet at a point on the negative voltage axis at Vce=-Va, the **early voltage**.
- The slope of the curves indicates that the output resistance looking into the collector is finite. The resistance is not critical in the dc analysis.

$$\frac{1}{r_o} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{v_{BE}=const.}$$

$$r_o \cong \frac{V_A}{I_C},$$

I_C : the quiescent collector current

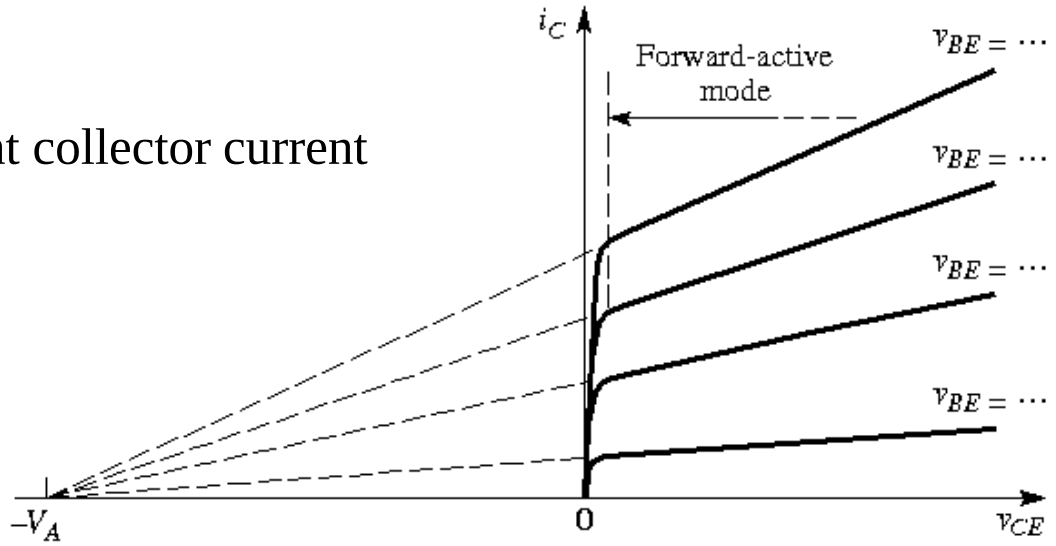


Figure 3.14 Current–voltage characteristics for the common-emitter circuit, showing the Early voltage

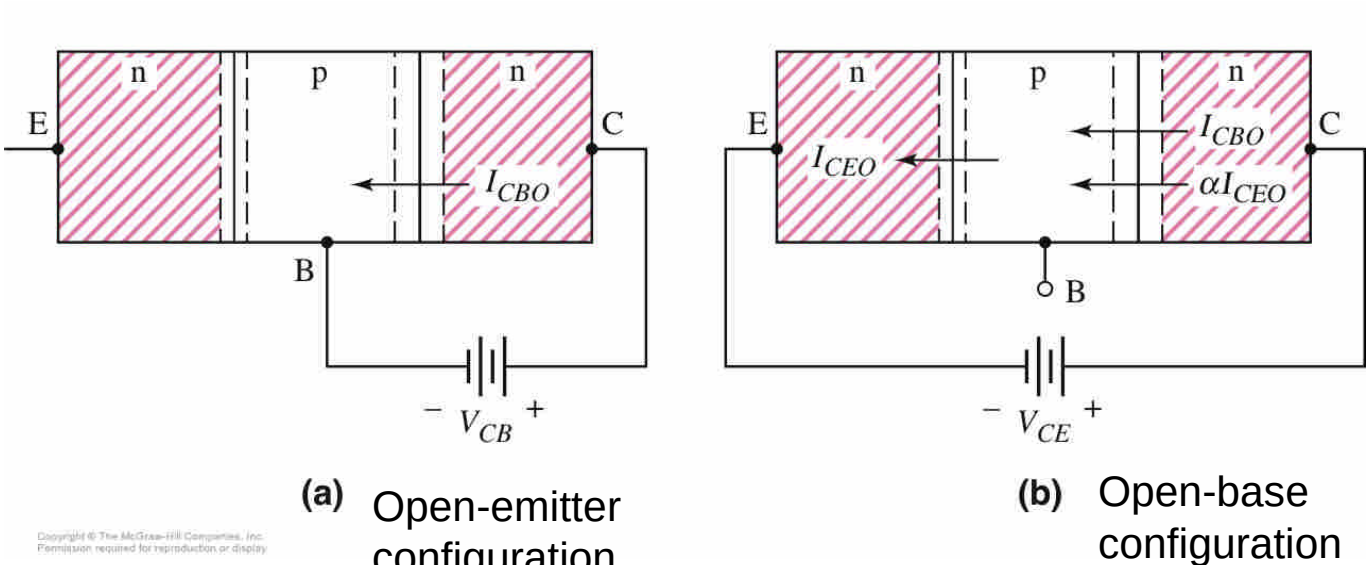
Leakage Currents

I_{CBO} : the normal leakage current in the reverse-biased BC pn junction

I_{CEO} : the BE current which is is induced by the forward-biased BE pn junction

$$I_{CEO} = \alpha I_{CEO} + I_{CBO}$$

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} = (1+\beta) I_{CBO}$$



(a) Open-emitter configuration

(b) Open-base configuration

Breakdown Voltage

- Common-Base Characteristics
  For the curves in which $i_E > 0$, breakdown begins earlier. The carriers flowing across the junction initiates the breakdown avalanche process at somewhat lower voltages.

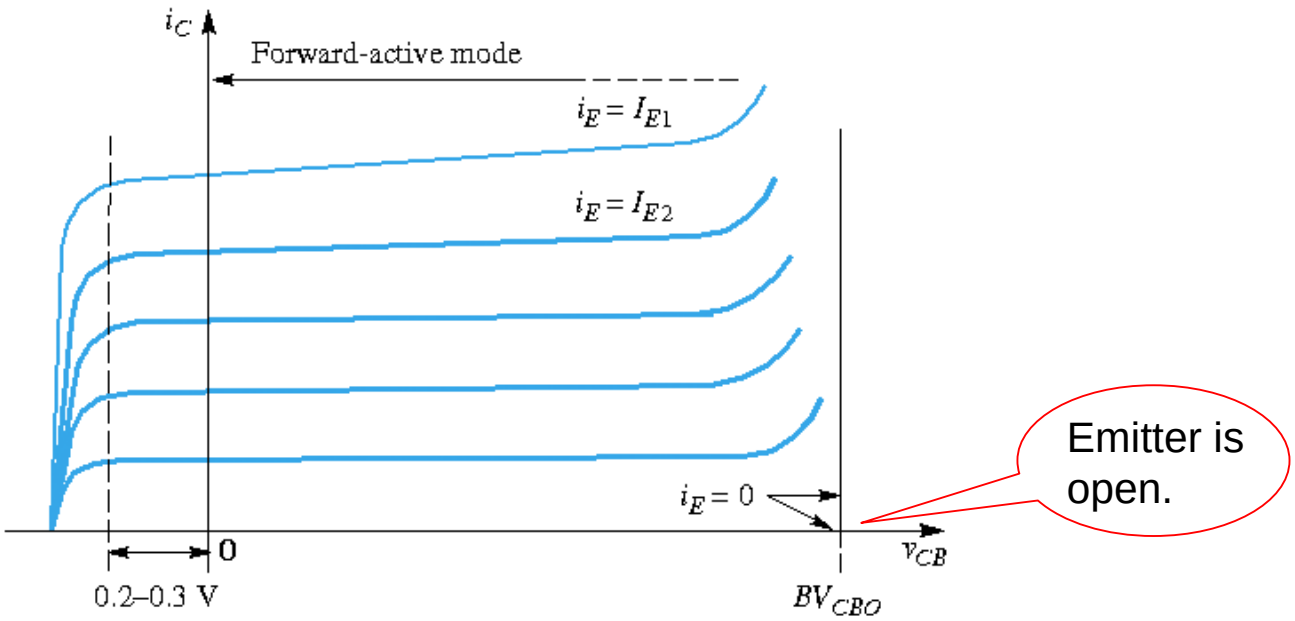


Figure 3.16 The i_C versus v_{CB} common-base characteristics, showing the collector–base junction breakdown

Breakdown Voltage

- Common-Emitter Characteristics

$$BV_{CEO} < BV_{CBO},$$

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}}, n = 3 \sim 6$$

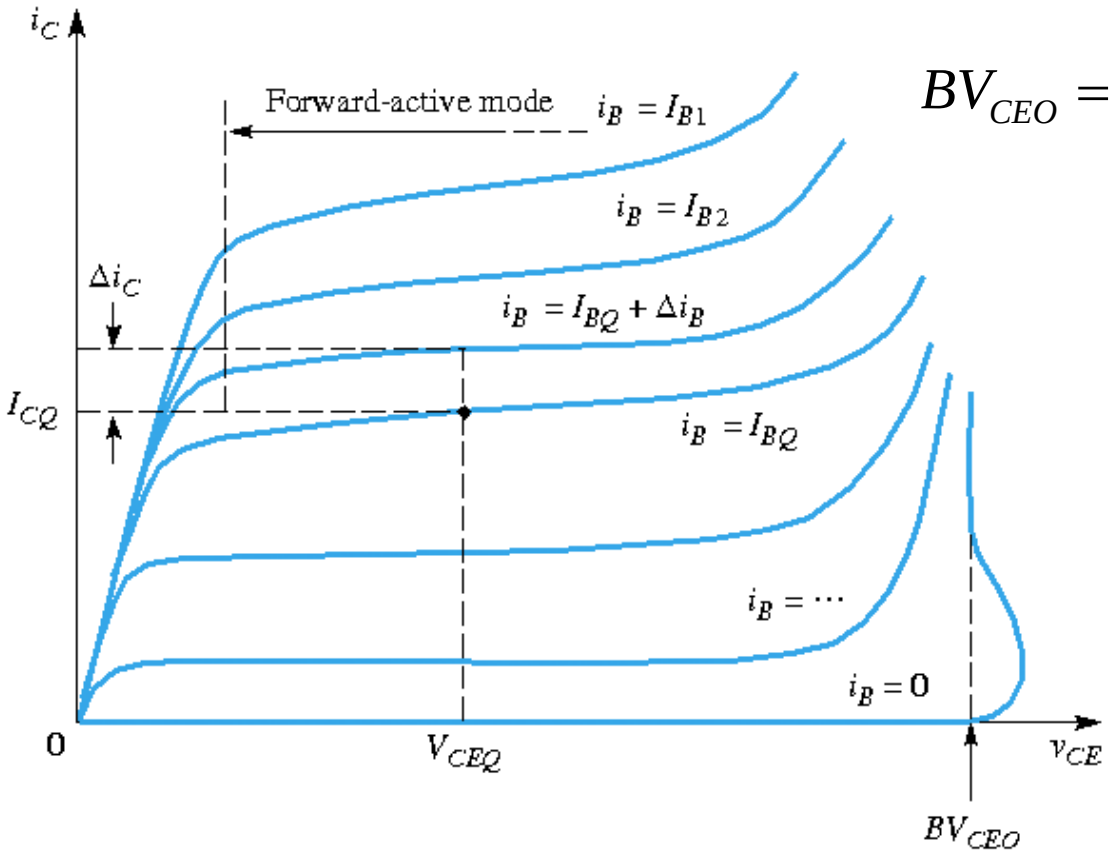


Figure 3.17 Common-emitter characteristics showing breakdown effects

DC Analysis of Common-Emitter Circuit for NPN

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} \quad \text{and} \quad I_C = \beta I_B$$

$$V_{CC} = I_C R_C + V_{CE} \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C$$

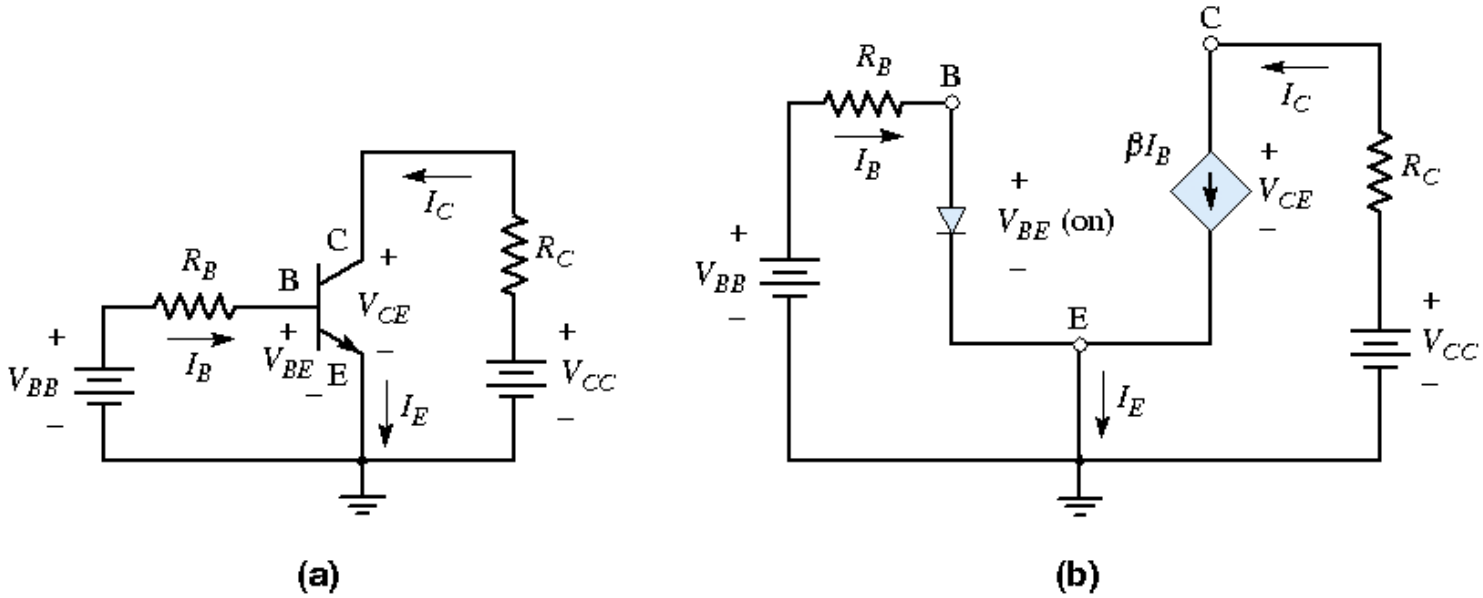
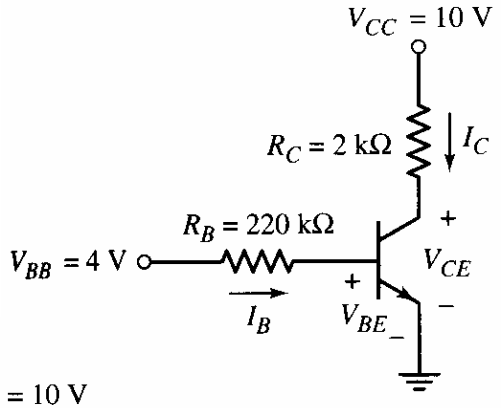


Figure 3.18 (a) Common-emitter circuit with an npn transistor and (b) dc equivalent circuit, with piecewise linear parameters

Example 3.3 **Objective:** Calculate the base, collector, and emitter currents and the C–E voltage for a common-emitter circuit.

For the circuit shown in Figure 3.18(a), the parameters are: $V_{BB} = 4\,\text{V}$, $R_B = 220\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $V_{CC} = 10\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 200$. Figure 3.19(a) shows the circuit without explicitly showing the voltage sources.



(a)

Solution: Referring to Figure 3.19(b), the base current is found as

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{4 - 0.7}{220} \Rightarrow 15\,\mu\text{A}$$

The collector current is

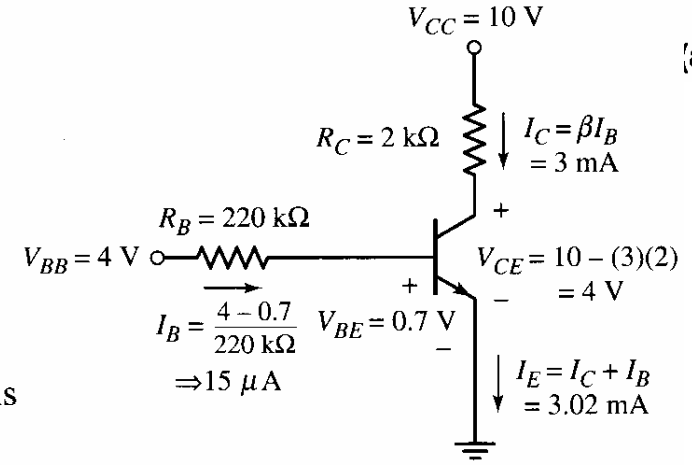
$$I_C = \beta I_B = (200)(15\,\mu\text{A}) \Rightarrow 3\,\text{mA}$$

and the emitter current is

$$I_E = (1 + \beta) \cdot I_B = (201)(15\,\mu\text{A}) \Rightarrow 3.02\,\text{mA}$$

From Equation (3.23(b)), the collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3)(2) = 4\,\text{V}$$



(b)

Comment: Since $V_{BB} > V_{BE}(\text{on})$ and $V_{CE} > V_{BE}(\text{on})$, the transistor is indeed biased in the forward-active mode. As a note, in an actual circuit, the voltage across a B–E junction may not be exactly 0.7 V, as we have assumed using the piecewise linear approximation. This may lead to slight inaccuracies between the calculated currents and voltages and the measured values. Also note that, if we take the difference between I_E and I_C, which is the base current, we obtain $I_B = 20\,\mu\text{A}$ rather than $15\,\mu\text{A}$. The difference is the result of roundoff error in the emitter current.

DC Analysis of Common-Emitter Circuit for PNP

$$I_B = \frac{V_{BB} - V_{EB}(\text{on})}{R_B} \text{ and } I_C = \beta I_B$$

$$V_{EC} = V_{CC} - I_C R_C$$

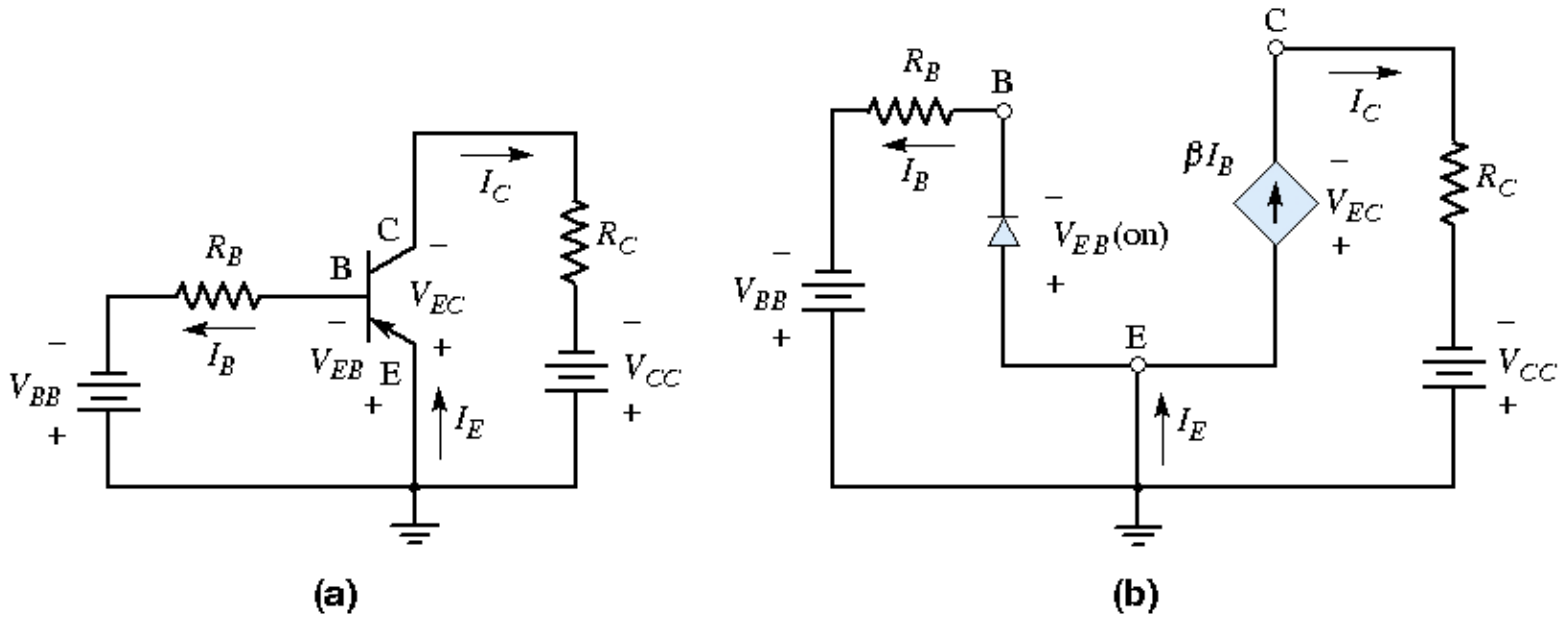
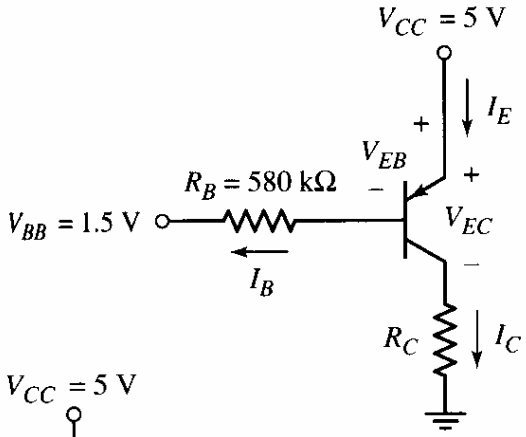


Figure 3.20 (a) Common-emitter circuit with a pnp transistor and (b) dc equivalent circuit using piecewise linear parameters

Example 3.4 **Objective:** Analyze the common-emitter circuit with a pnp transistor.

For the circuit shown in Figure 3.21(a), the parameters are: $V_{BB} = 1.5\,\text{V}$, $R_B = 580\,\text{k}\Omega$, $V_{CC} = 5\,\text{V}$, $V_{EB}(\text{on}) = 0.6\,\text{V}$, and $\beta = 100$. Find I_B, I_C, I_E, and R_C such that $V_{EC} = (\frac{1}{2})V_{CC}$.



Solution: Writing a Kirchhoff voltage law equation around the E–B loop, we find the base current to be

$$I_B = \frac{V_{CC} - V_{EB}(\text{on}) - V_{BB}}{R_B} = \frac{5 - 0.6 - 1.5}{580} \Rightarrow 5\,\mu\text{A}$$

The collector current is

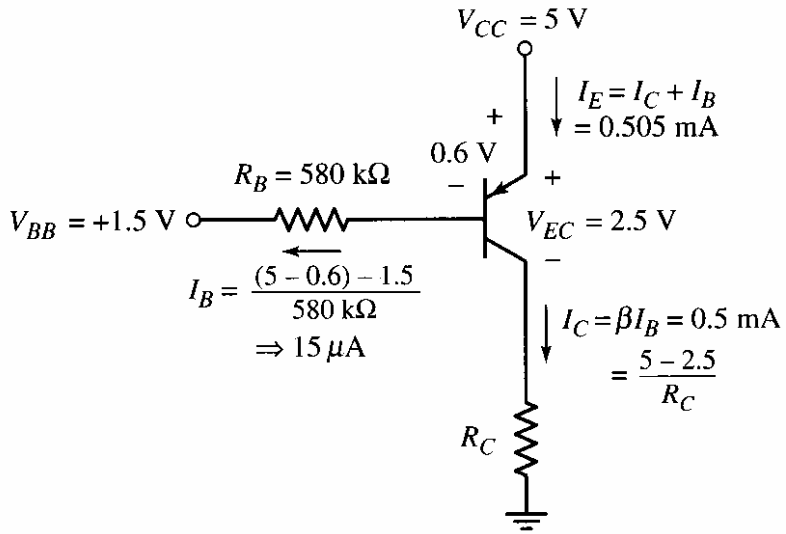
$$I_C = \beta I_B = (100)(5\,\mu\text{A}) \Rightarrow 0.5\,\text{mA}$$

and the emitter current is

$$I_E = (1 + \beta)I_B = (101)(5\,\mu\text{A}) \Rightarrow 0.505\,\text{mA}$$

For a C–E voltage of $V_{EC} = \frac{1}{2}V_{CC} = 2.5\,\text{V}$, R_C is

$$R_C = \frac{V_{CC} - V_{EC}}{I_C} = \frac{5 - 2.5}{0.5} = 5\,\text{k}\Omega$$



Comment: In this case, the difference between V_{CC} and V_{BB} is greater than the transistor turn-on voltage, or $(V_{CC} - V_{BB}) > V_{EB}(\text{on})$. Also, because $V_{EC} > V_{EB}(\text{on})$, the pnp bipolar transistor is biased in the forward-active mode.

Discussion: In this example, we used an emitter-base turn-on voltage of $V_{EB}(\text{on}) = 0.6\,\text{V}$, whereas previously we used a value of 0.7 V. We must keep in mind that the turn-on voltage is an approximation and the actual base–emitter voltage will depend on the type of transistor used and the current level. In most situations, choosing a value of 0.6 V or 0.7 V will make only minor differences. However, most people tend to use the value of 0.7 V.

Load Line

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = 5 - \frac{V_{CE}}{2}$$

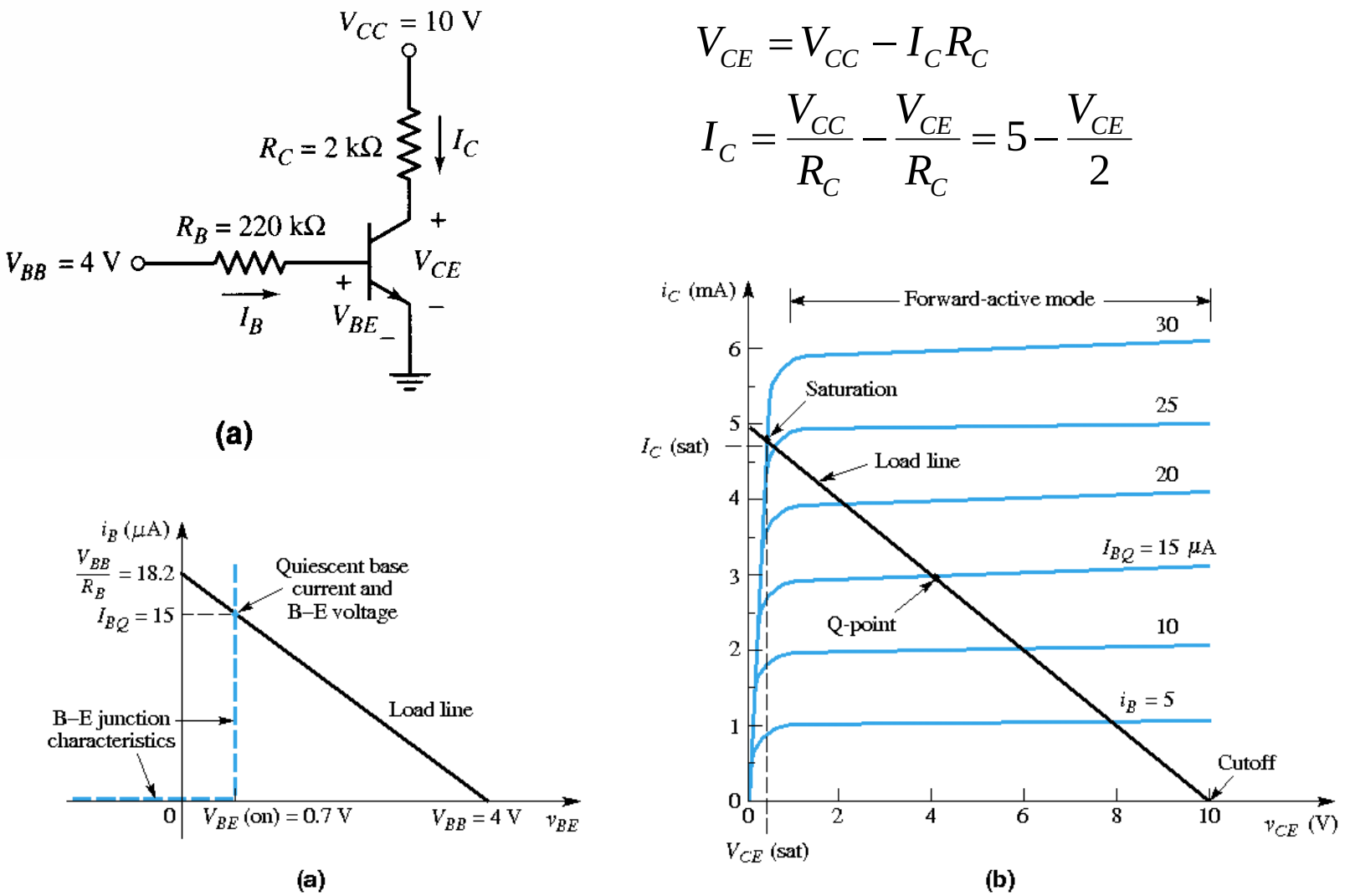


Figure 3.22 (a) Base–emitter junction characteristics and the input load line and (b) common-emitter transistor characteristics and the collector–emitter load line

Example 3.5 **Objective:** Calculate the currents and voltages in a circuit when the transistor is driven into saturation.

For the circuit shown in Figure 3.23, the transistor parameters are: $\beta = 100$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$. If the transistor is biased in saturation, assume $V_{CE}(\text{sat}) = 0.2\,\text{V}$.

Solution: Since +8 V is applied to the input side of R_B, the base–emitter junction is certainly forward biased, so the transistor is turned on. The base current is

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{9 - 0.7}{220} \Rightarrow 33.2\,\mu\text{A}$$

If we first assume that the transistor is biased in the active region, then the collector current is

$$I_C = \beta I_B = (100)(33.2\,\mu\text{A}) \Rightarrow 3.32\,\text{mA}$$

The collector–emitter voltage is then

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3.32)(4) = -3.28\,\text{V}$$

However, the collector–emitter voltage of the npn transistor in the common-emitter configuration shown in Figure 3.23(a) cannot be negative. Therefore, our initial assumption of the transistor being biased in the forward-active mode is incorrect. Instead, the transistor must be biased in saturation.

As given in the "objective" statement, set $V_{CE}(\text{sat}) = 0.2\,\text{V}$. The collector current is

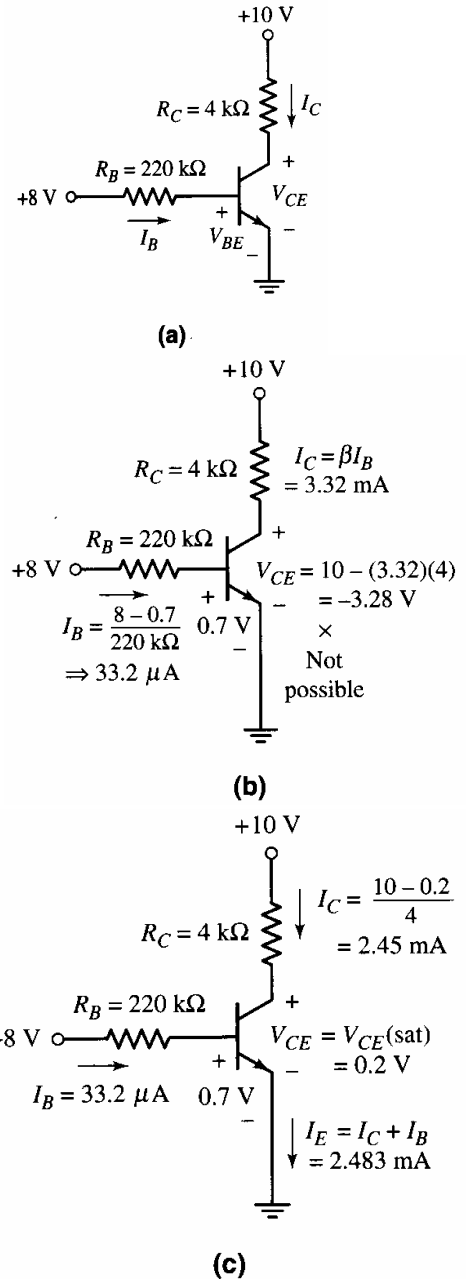
$$I_C = I_C(\text{sat}) = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} = \frac{10 - 0.2}{4} = 2.45\,\text{mA}$$

Assuming that the B–E voltage is still equal to $V_{BE}(\text{on}) = 0.7\,\text{V}$, the base current is $I_B = 33.2\,\mu\text{A}$, as previously determined. If we take the ratio of collector current to base current, then

$$\frac{I_C}{I_B} = \frac{2.45}{0.0332} = 74 < \beta$$

The emitter current is

$$I_E = I_C + I_B = 2.45 + 0.033 = 2.48\,\text{mA}$$



Bipolar DC Analysis Technique

Analyzing the dc response of a bipolar transistor circuit requires knowing the mode of operation of the transistor. In some cases, the mode of operation may not be obvious, which means that we have to guess the state of the transistor, then analyze the circuit to determine if we have a solution consistent with our initial guess. To do this, we can:

1. Assume that the transistor is biased in the forward-active mode in which case $V_{BE} = V_{BE}(\text{on})$, $I_B > 0$, and $I_C = \beta I_B$.
2. Analyze the "linear" circuit with this assumption.
3. Evaluate the resulting state of the transistor. If the initial assumed parameter values and $V_{CE} > V_{CE}(\text{sat})$ are true, then the initial assumption is correct. However, if $I_B < 0$, then the transistor is probably cut off, and if $V_{CE} < 0$, the transistor is likely biased in saturation.
4. If the initial assumption is proven incorrect, then a new assumption must be made and the new "linear" circuit must be analyzed. Step 3 must then be repeated.

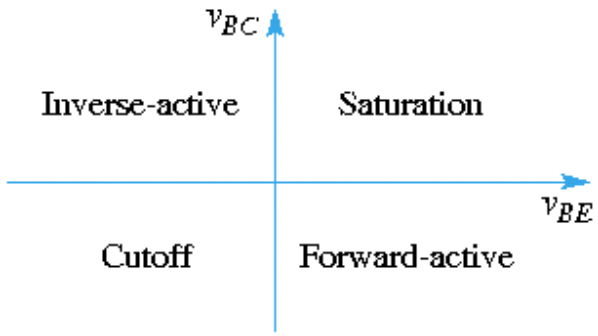


Figure 3.24 Bias conditions for the four modes of operation of an npn transistor

Voltage Transfer Characteristics

EXAMPLE 5.6

Objective: Develop the voltage transfer curves for the circuits shown in Figures 5.27(a) and 5.27(b).

Assume npn transistor parameters of $V_{BE}(\text{on}) = 0.7$ V, $\beta = 120$, $V_{CE}(\text{sat}) = 0.2$ V, and $V_A = \infty$, and pnp transistor parameters of $V_{EB}(\text{on}) = 0.7$ V, $\beta = 80$, $V_{EC}(\text{sat}) = 0.2$ V, and $V_A = \infty$.

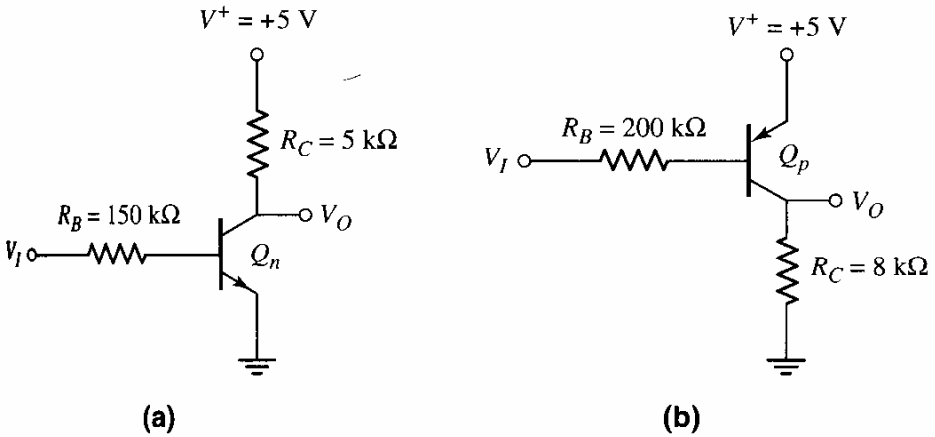


Figure 5.27 Circuits for Example 5.6; (a) npn circuit and (b) pnp circuit

Solution (npn transistor circuit): For $V_I \leq 0.7$ V, the transistor Q_n is cut off, so that $I_B = I_C = 0$. The output voltage is then $V_O = V^+ = 5$ V.

For $V_I > 0.7$ V, the transistor Q_n turns on and is initially biased in the forward-active mode. We have

$$I_B = \frac{V_I - 0.7}{R_B}$$

and

$$I_C = \beta I_B = \frac{\beta(V_I - 0.7)}{R_B}$$

Then

$$V_O = 5 - I_C R_C = 5 - \frac{\beta(V_I - 0.7)R_C}{R_B}$$

This equation is valid for $0.2 \leq V_O \leq 5$ V. When $V_O = 0.2$ V, the transistor Q_n goes into saturation. When $V_O = 0.2$ V, the input voltage is found from

$$0.2 = 5 - \frac{(120)(V_I - 0.7)(5)}{150}$$

which yields $V_I = 1.9$ V. For $V_I \geq 1.9$ V, the transistor Q_n remains biased in the saturation region.

The voltage transfer curve is shown in Figure 5.28(a).

Solution (pnp transistor circuit): For $4.3 \leq V_I \leq 5$ V, the transistor Q_p is cut off, so that $I_B = I_C = 0$. The output voltage is then $V_O = 0$.

For $V_I < 4.3$ V, the transistor Q_p turns on and is biased in the forward-active mode. We have

$$I_B = \frac{(5 - 0.7) - V_I}{R_B}$$

and

$$I_C = \beta I_B = \beta\left[\frac{(5 - 0.7) - V_I}{R_B}\right]$$

The output voltage is then

$$V_O = I_C R_C = \beta R_C\left[\frac{(5 - 0.7) - V_I}{R_B}\right]$$

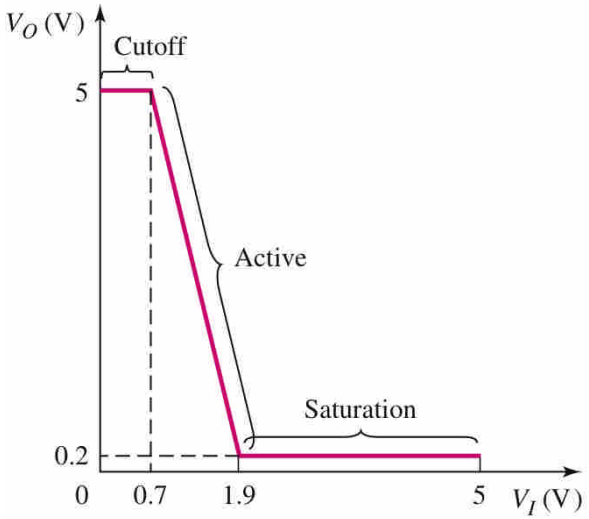
This equation is valid for $0 \leq V_O \leq 4.8$ V. When $V_O = 4.8$ V, the transistor Q into saturation.

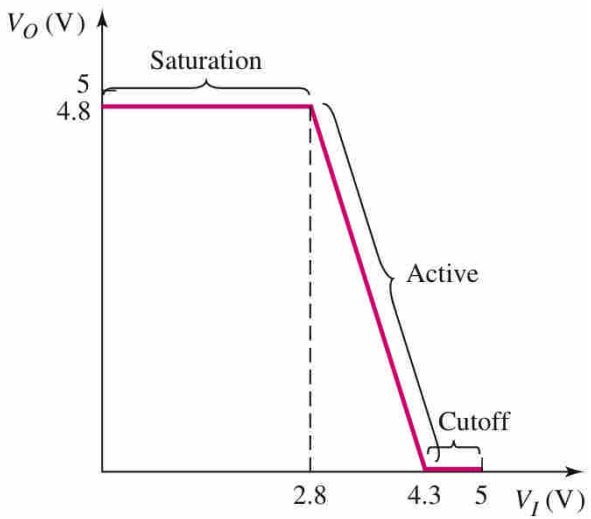
When $V_O = 4.8$ V, the input voltage is found from

$$4.8 = (80)(8)\left[\frac{(5 - 0.7) - V_I}{200}\right]$$

which yields $V_I = 2.8$ V. For $V_I \leq 2.8$ V, the transistor Q_p remains biased in uration mode.

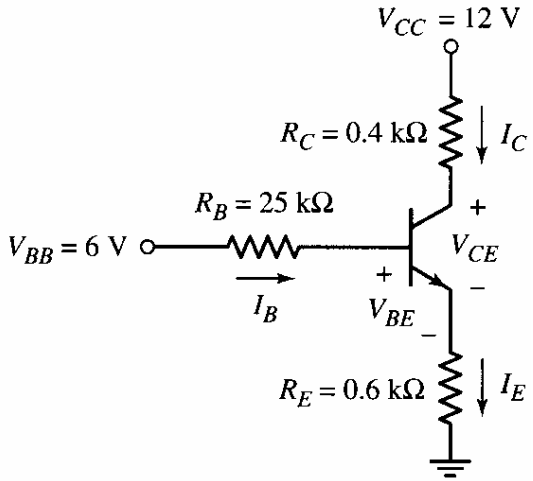
The voltage transfer curve is shown in Figure 5.28(b).





Example 3.6 **Objective:** Calculate the characteristics of a circuit containing an emitter resistor.

For the circuit shown in Figure 3.26(a), let $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $\beta = 75$.



Solution:

***Q*-Point Values:**

Writing the Kirchhoff's voltage law equation around the B–E loop, we have

$$V_{BB} = I_B R_B + V_{BE}(\text{on}) + I_E R_E \tag{3.29}$$

Assuming the transistor is biased in the forward-active mode, we can write $I_E = (1 + \beta)I_B$. We can then solve Equation (3.29) for the base current:

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B + (1 + \beta)R_E} = \frac{6 - 0.7}{25 + (76)(0.6)} \Rightarrow 75.1\,\mu\text{A}$$

The collector and emitter currents are

$$I_C = \beta I_B = (75)(75.1\,\mu\text{A}) \Rightarrow 5.63\,\text{mA}$$

and

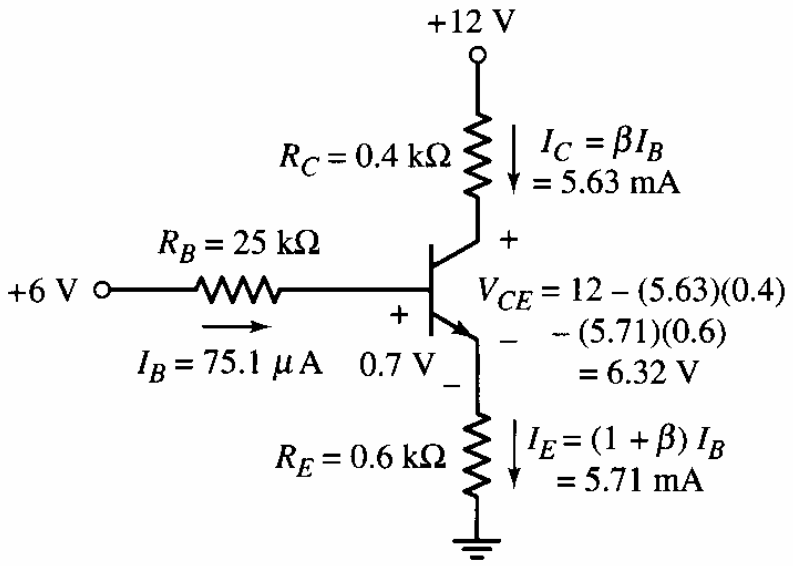
$$I_E = (1 + \beta)I_B = (76)(75.1\,\mu\text{A}) \Rightarrow 5.71\,\text{mA}$$

Referring to Figure 3.26(b), the collector–emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 12 - (5.63)(0.4) - (5.71)(0.6)$$

or

$$V_{CE} = 6.32\,\text{V}$$



Load Line:

We again use Kirchhoff's voltage law around the C–E loop. From the relationship between the collector and emitter currents, we find

$$V_{CE} = V_{CC} - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right] = 12 - I_C\left[0.4 + \left(\frac{76}{75}\right)(0.6)\right]$$

or

$$V_{CE} = 12 - I_C(1.01)$$

The load line and the calculated Q-point are shown in Figure 3.27. A few transistor characteristics of I_C versus V_{CE} are superimposed on the figure.

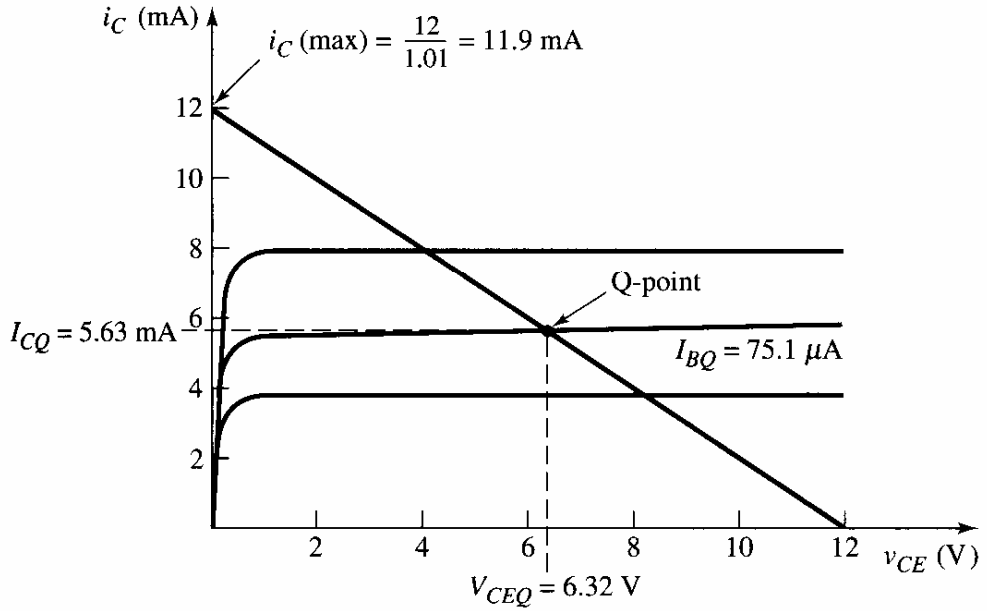
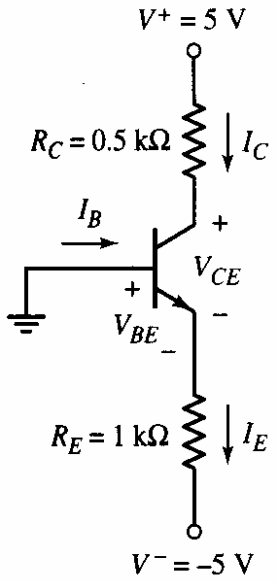


Figure 3.27 Load line for the circuit in Figure 3.26

Example 3.7 **Objective:** Calculate the characteristics of a circuit containing both a positive and a negative power supply voltage.

For the circuit shown in Figure 3.28, let $V_{BE}(\text{on}) = 0.65\,\text{V}$ and $\beta = 100$. Even though the base is at ground potential, the B–E junction is forward biased through R_E and V^-.



Solution:

***Q*-Point Values:**

Writing the Kirchhoff's voltage law equation around the B–E loop, we have

$$0 = V_{BE}(\text{on}) + I_E R_E + V^-$$

which yields

$$I_E = \frac{-V^- - V_{BE}(\text{on})}{R_E} = \frac{-(-5) - 0.65}{1} = 4.35\,\text{mA}$$

The base current is

$$I_B = \frac{I_E}{1+\beta} = \frac{4.35}{101} \Rightarrow 43.1\,\mu\text{A}$$

and the collector current is

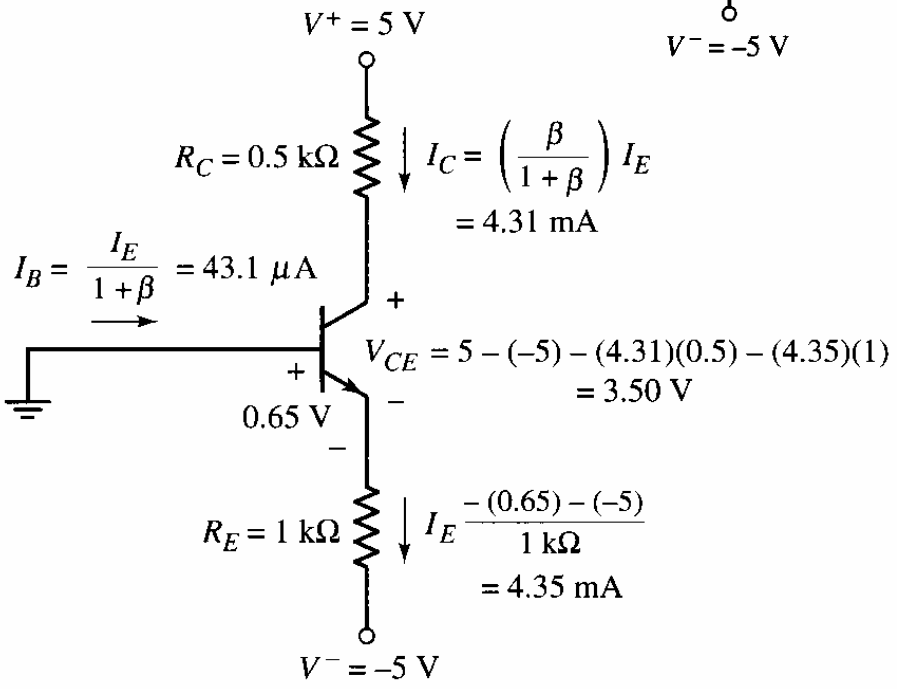
$$I_C = \left(\frac{\beta}{1+\beta}\right) I_E = \left(\frac{100}{101}\right) \cdot (4.35) = 4.31\,\text{mA}$$

Referring to Figure 3.28(b), the C–E voltage is

$$V_{CE} = V^+ - I_C R_C - I_E R_E - V^-$$

or

$$V_{CE} = 5 - (4.31)(0.5) - (4.35)(1) - (-5) = 3.50\,\text{V}$$



Load Line:
The load line equation is

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right] = (5-(-5)) - I_C\left[0.5 + \left(\frac{101}{100}\right)(1)\right]$$

or

$$V_{CE} = 10 - I_C(1.51)$$

The load line and the calculated Q-point are shown in Figure 3.29.

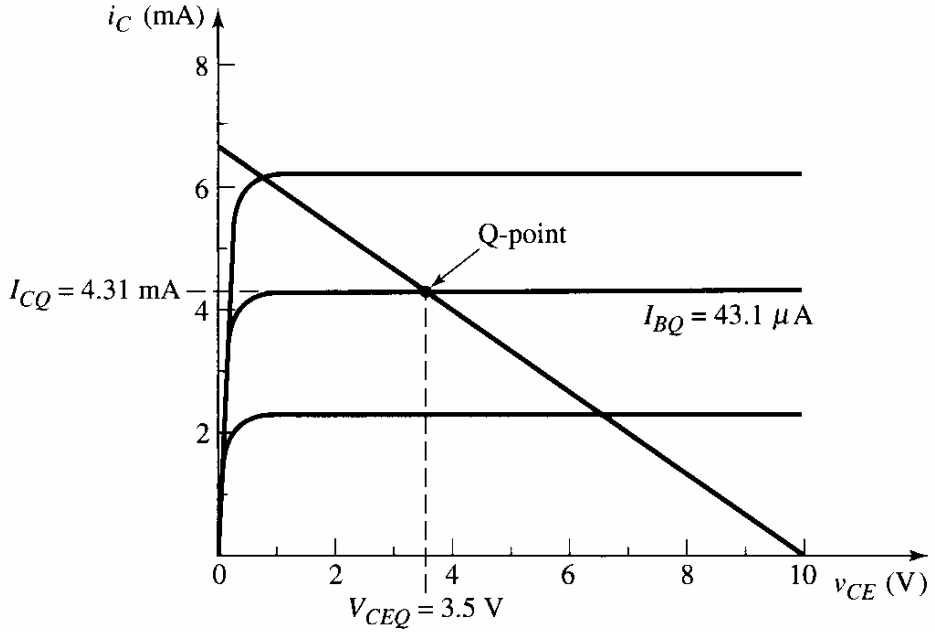


Figure 3.29 Load line for the circuit in Figure 3.28

DESIGN EXAMPLE 5.9

Objective: Design the common-base circuit shown in Figure 5.35 such that $I_{EQ} = 0.50$ mA and $V_{ECQ} = 4.0$ V.

Assume transistor parameters of $\beta = 120$ and $V_{EB}(\text{on}) = 0.7$ V.

Solution: Writing Kirchhoff's voltage law equation around the base–emitter loop (assuming the transistor is biased in the forward-active mode), we have

$$V^+ = I_{EQ}R_E + V_{EB}(\text{on}) + \left(\frac{I_{EQ}}{1+\beta}\right)R_B$$

or

$$5 = (0.5)R_E + 0.7 + \left(\frac{0.5}{121}\right)(10)$$

which yields

$$R_E = 8.52\ \text{k}\Omega$$

We can find

$$I_{CQ} = \left(\frac{\beta}{1+\beta}\right)I_{EQ} = \left(\frac{120}{121}\right)(0.5) = 0.496\ \text{mA}$$

Now, writing Kirchhoff's voltage law equation around the emitter–collector loop, we have

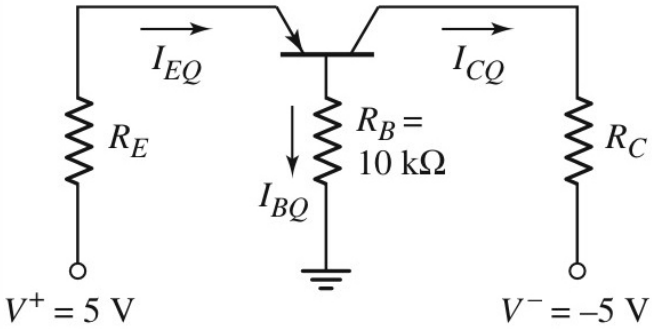
$$V^+ = I_{EQ}R_E + V_{ECQ} + I_{CQ}R_C + V^-$$

or

$$5 = (0.5)(8.52) + 4 + (0.496)R_C + (-5)$$

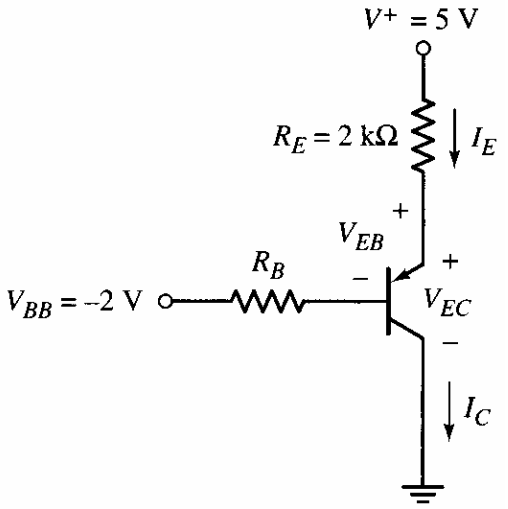
which yields

$$R_C = 3.51\ \text{k}\Omega$$



Design Example 3.8 **Objective:** Design a pnp bipolar transistor circuit.

For the circuit shown in Figure 3.33(a), let $V_{EB}(\text{on}) = 0.6\,\text{V}$ and $\beta = 60$. Design the circuit such that $V_{ECQ} = 2.5\,\text{V}$.



Solution:

***Q*-Point Values:**

Writing the Kirchhoff's voltage law equation around the E–C loop, we obtain

$$V^+ = I_E R_E + V_{EC}$$

or

$$5 = I_E(2) + 2.5$$

which yields $I_E = 1.25\,\text{mA}$. The collector current is

$$I_C = [\beta/(1+\beta)]I_E = [(60)/61](1.25) = 1.23\,\text{mA}$$

The base current is

$$I_B = I_E/(1+\beta) = 1.25/61 = 0.0205\,\text{mA}$$

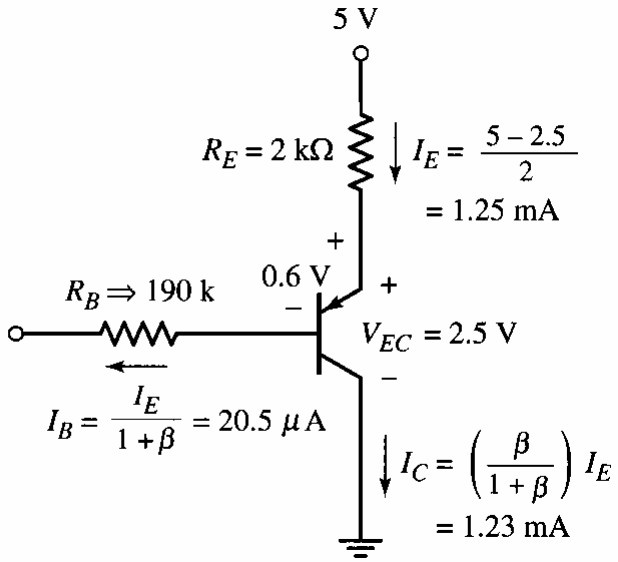
Writing the Kirchhoff's voltage law equation around the E–B loop, we find

$$V^+ = I_E R_E + V_{EB}(\text{on}) + I_B R_B + V_{BB}$$

or

$$5 = (1.25)(2) + 0.6 + (0.0205)R_B + (-2)$$

which yields $R_B = 190\,\text{k}\Omega$.



Load Line:
The load line equation is

$$V_{EC} = V^+ - I_E R_E = V^+ - I_C\left(\frac{1+\beta}{\beta}\right)R_E$$

or

$$V_{EC} = 5 - I_C\left(\frac{61}{60}\right)(2) = 5 - I_C(2.03)$$

The load line and calculated Q-point are shown in Figure 3.34.

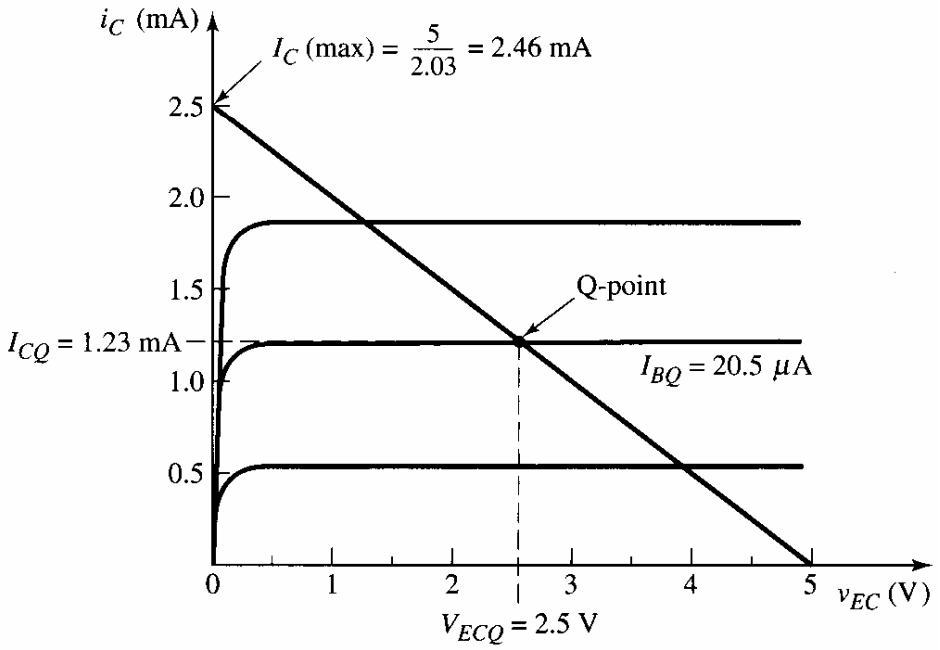


Figure 3.34 Load line for the circuit in Figure 3.33

Example 3.9 **Objective:** Calculate the characteristics of an npn bipolar circuit with a load resistance. The load resistance can represent a second transistor stage connected to the output of a transistor circuit.

For the circuit shown in Figure 3.36(a), the transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 100$.

Solution:

***Q*-Point Values:**

Kirchhoff's voltage law equation around the B–E loop yields

$$I_B R_B + V_{BE}(\text{on}) + I_E R_E + V^- = 0$$

Again assuming $I_E = (1+\beta)I_B$, we find

$$I_B = \frac{-(V^- + V_{BE}(\text{on}))}{R_B + (1+\beta)R_E} = \frac{-(-5+0.7)}{10+(101)(5)} \Rightarrow 8.35\,\mu\text{A}$$

The collector and emitter currents are

$$I_C = \beta I_B = (100)(8.35\,\mu\text{A}) \Rightarrow 0.835\,\text{mA}$$

and

$$I_E = (1+\beta)I_B = (101)(8.35\,\mu\text{A}) \Rightarrow 0.843\,\text{mA}$$

At the collector node, we can write

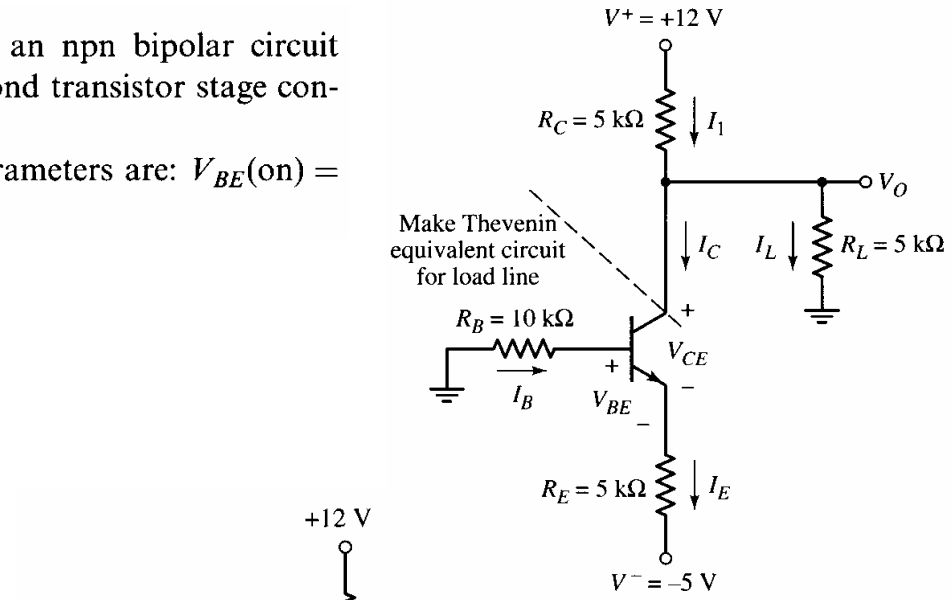
$$I_C = I_1 - I_L = \frac{V^+ - V_O}{R_C} - \frac{V_O}{R_L}$$

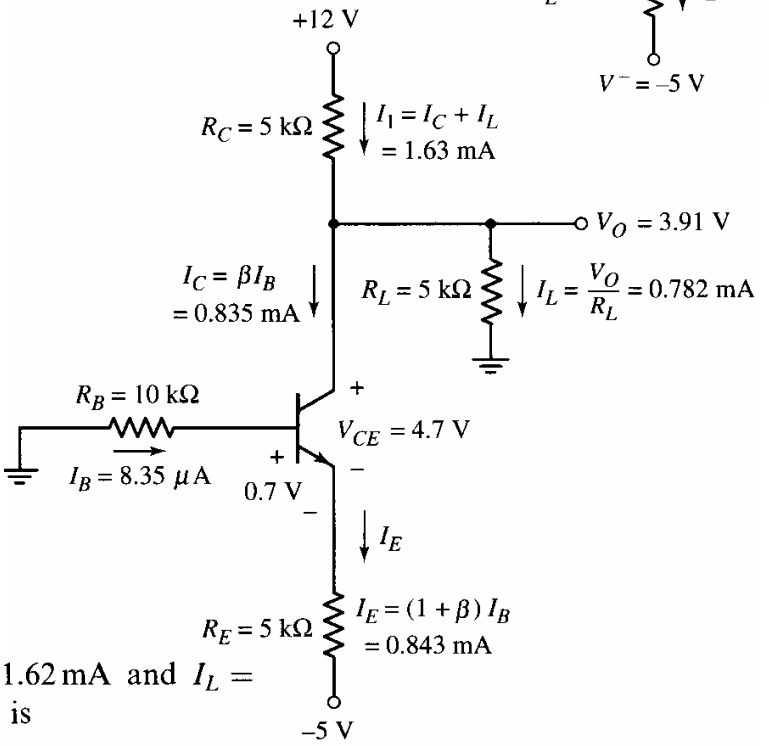
or

$$0.835 = \frac{12 - V_O}{5} - \frac{V_O}{5}$$

Solving for V_O, we get $V_O = 3.91\,\text{V}$. The currents are then $I_1 = 1.62\,\text{mA}$ and $I_L = 0.782\,\text{mA}$. Referring to Figure 3.36(b), the collector–emitter voltage is

$$V_{CE} = V_O - I_E R_E - (-5) = 3.91 - (0.843)(5) - (-5) = 4.70\,\text{V}$$





Load Line:

The load line equation for this circuit is not as straightforward as for previous circuits. The easiest approach to finding the load line is to make a "Thevenin equivalent circuit" of R_L, R_C, and V^+, as indicated in Figure 3.36(a). (Thevenin equivalent circuits are also covered later in this chapter, in Section 3.4.) The Thevenin equivalent resistance is

$$R_{TH} = R_L \| R_C = 5 \| 5 = 2.5\,\text{k}\Omega$$

and the Thevenin equivalent voltage is

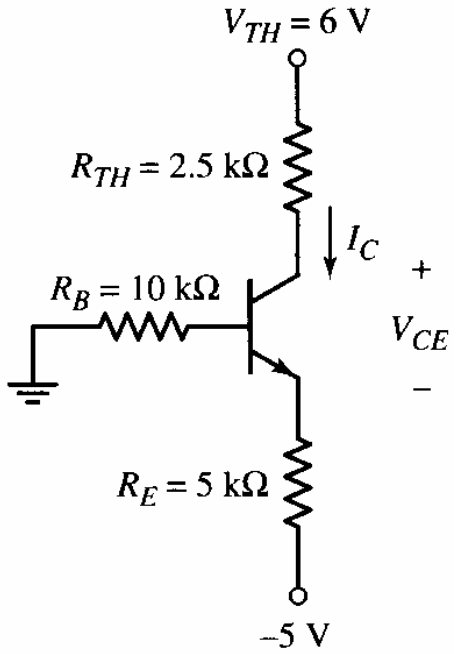
$$V_{TH} = \left(\frac{R_L}{R_L + R_C}\right) \cdot V^+ = \left(\frac{5}{5+5}\right) \cdot (12) = 6\,\text{V}$$

The equivalent circuit is shown in Figure 3.36(c). The Kirchhoff voltage law equation around the C–E loop is

$$V_{CE} = (6 - (-5)) - I_C R_{TH} - I_E R_E = 11 - I_C(2.5) - I_C\left(\frac{101}{100}\right) \cdot (5)$$

or

$$V_{CE} = 11 - I_C(7.55)$$



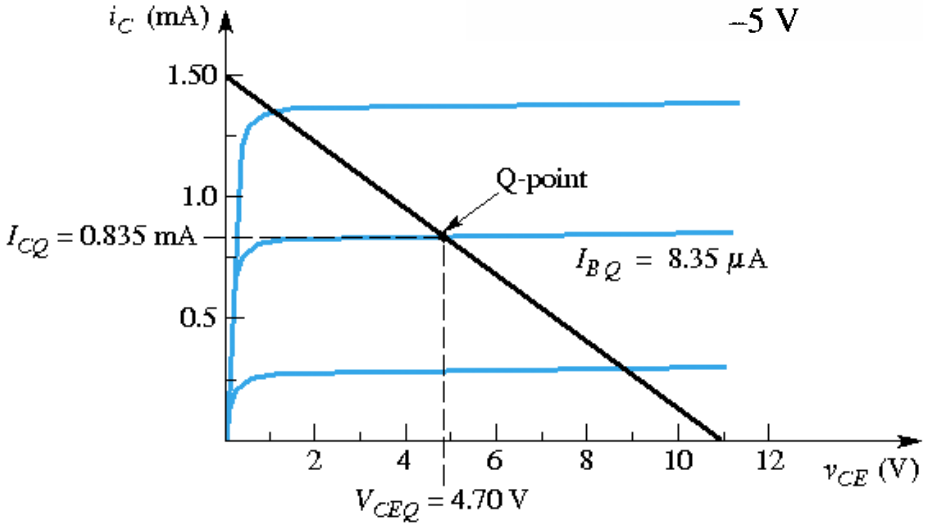


Figure 3.37 Load line for the circuit in Figure 3.36(a)

Transistor Circuit Application: Switch

- Cutoff and Saturation

Cutoff:

$$v_I < V_{BE}(on),\ i_B = i_C = 0$$
$$v_O = V_{CC}$$

Saturation:

$$v_I = V_{CC},\quad R_B / R_C < \beta$$
$$v_O = V_{CE}(sat)$$

$$i_B \cong \frac{v_I - V_{BE}(on)}{R_B}$$

$$i_c = I_C(sat) = \frac{V_{CC} - V_{CE}(sat)}{R_C}$$

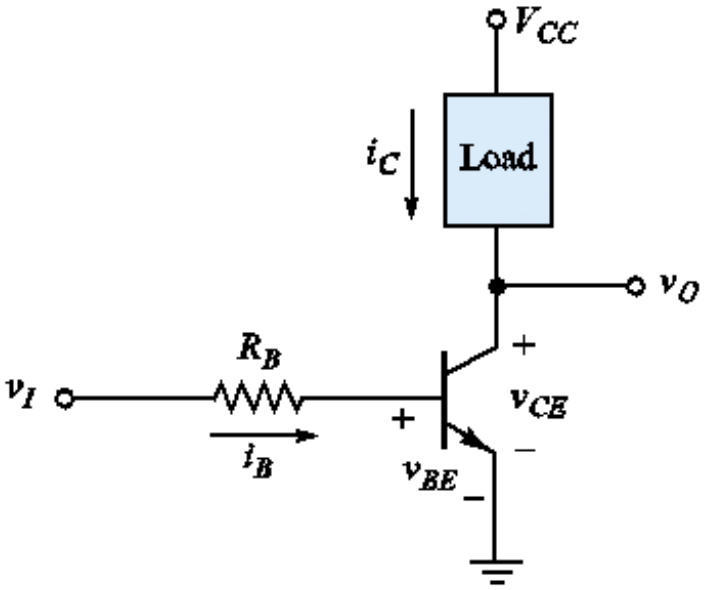


Figure 3.42 An npn bipolar inverter circuit used as a switch

EXAMPLE **5.12**

Objective: Calculate the resistances R and R_B, and power dissipated in the transistor for the bipolar inverter switch shown in Figure 5.49. The transistor is used to turn the light-emitting diode (LED) on and off. The required LED current is $I_C = 12$ mA to produce the specified output light.

Assume transistor parameters of $\beta = 50$, $V_{BE}(\text{on}) = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V, and assume the diode cut-in voltage is $V_\gamma = 1.5$ V. [*Note:* LEDs are fabricated with compound semiconductor materials and have a larger cut-in voltage compared to silicon diodes.]

Solution: For $v_I = 0$, the transistor is cut off so that $I_B = I_C = 0$ and the LED is also off.

For $v_I = 5$ V, we require $I_C = 12$ mA and want the transistor to be driven into saturation. Then

$$R = \frac{V^+ - (V_\gamma + V_{CE}(\text{sat}))}{I_C} = \frac{5 - (1.5 + 0.2)}{12}$$

or

$$R = 0.275\,\text{k}\Omega = 275\,\Omega$$

We may let $I_C/I_B = 20$. Then $I_B = 12/20 = 0.6$ mA. Now

$$R_B = \frac{v_I - V_{BE}(\text{on})}{I_B} = \frac{5 - 0.7}{0.6}$$

or

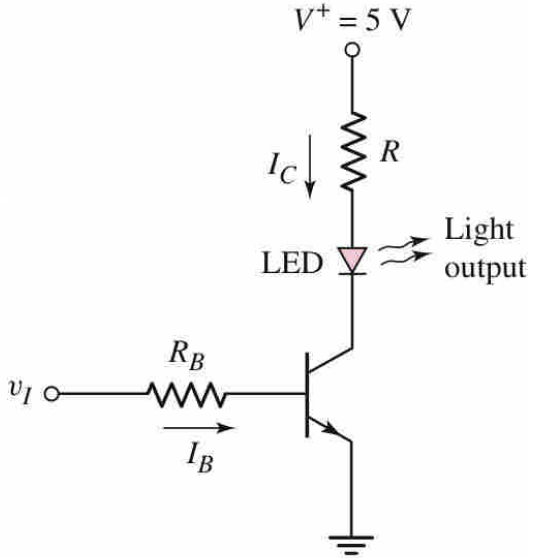
$$R_B = 7.17\,\text{k}\Omega$$

The power dissipated in the transistor is

$$P = I_B V_{BE}(\text{on}) + I_C V_{CE} = (0.6)(0.7) + (12)(0.2)$$

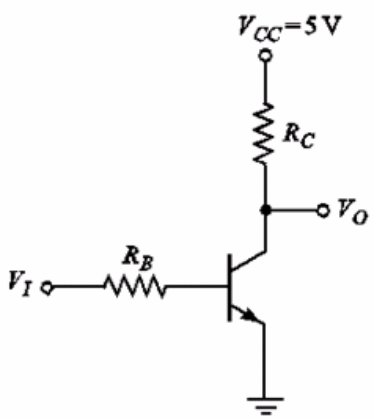
or

$$P = 2.82\,\text{mW}$$



Transistor Circuit Application: Digital Logic

- Bipolar Inverter



- Multiple-input NOR gate

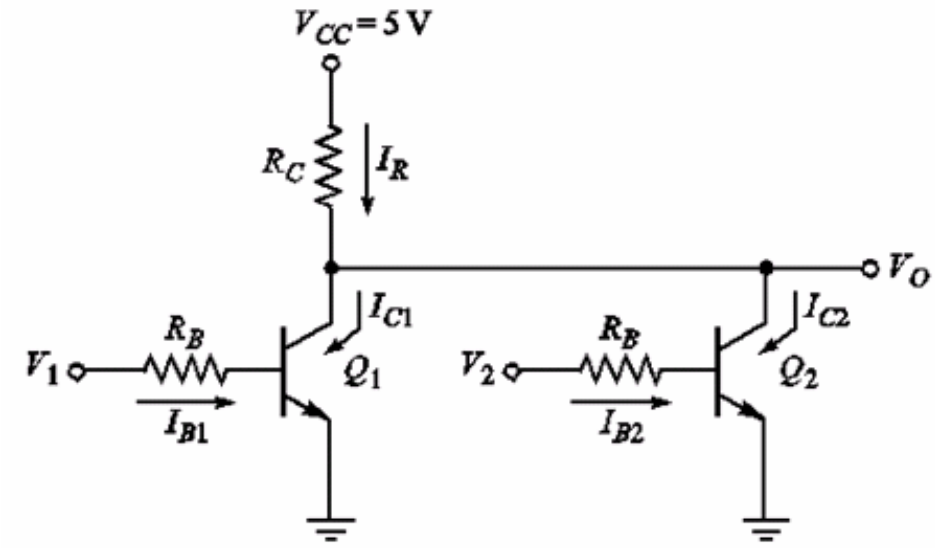
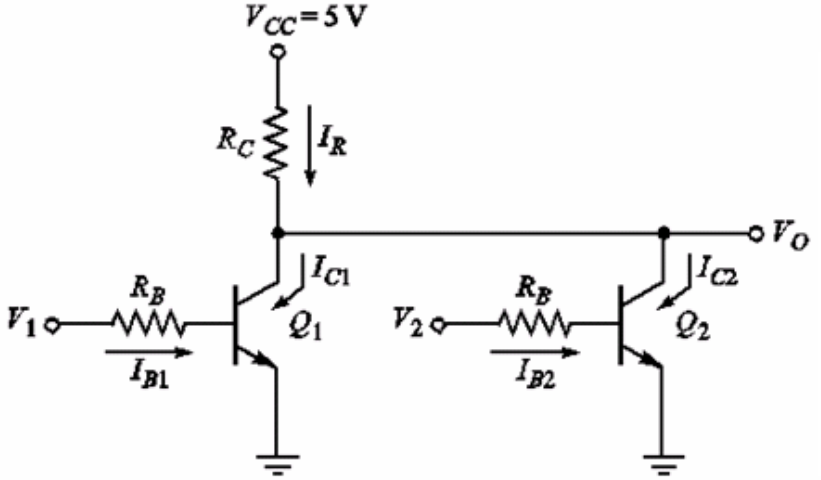


Table 3.2 The bipolar NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	5
5	0	0.2
0	5	0.2
5	5	0.2

Example 3.11 **Objective:** Determine the currents and voltages in the circuit shown in Figure 3.43(b).

Assume the transistor parameters are: $\beta = 50$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_{CE}(\text{sat}) = 0.2\,V$. Let $R_C = 1\,\text{k}\Omega$ and $R_B = 20\,\text{k}\Omega$. Determine the currents and output voltage for various input conditions.



Solution: The following table indicates the equations and results for this example.

Condition	V_O	I_R	Q_1	Q_2
$V_1 = 0$, $V_2 = 0$	5 V	0	$I_{B1} = I_{C1} = 0$	$I_{B2} = I_{C2} = 0$
$V_1 = 5\,\text{V}$, $V_2 = 0$	0.2 V	$\frac{5 - 0.2}{1} = 4.48\,\text{mA}$	$I_{B1} = \frac{5 - 0.7}{20} = 0.215\,\text{mA}$ $I_{C1} = I_R = 4.8\,\text{mA}$	$I_{B2} = I_{C2} = 0$
$V_1 = 0$, $V_2 = 5\,\text{V}$	0.2 V	4.8 mA	$I_{B1} = I_{C1} = 0$	$I_{B2} = 0.215\,\text{mA}$ $I_{C2} = I_R = 4.8\,\text{mA}$
$V_1 = 5\,\text{V}$, $V_2 = 5\,\text{V}$	0.2 V	4.8 mA	$I_{B1} = 0.215\,\text{mA}$ $I_{C1} = \frac{I_R}{2} = 2.4\,\text{mA}$	$I_{B2} = 0.215\,\text{mA}$ $I_{C2} = \frac{I_R}{2} = 2.4\,\text{mA}$

Transistor Circuit Application: Digital Logic

Example 3.12 **Objective:** Determine the dc voltage transfer characteristics and then the amplification factor of the circuit shown in Figure 3.44(a).

Assume the transistor parameters are: $\beta_F = 100$, $V_A = \infty$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_{CE}(\text{sat}) = 0.2\,\text{V}$.

DC Solution: For $v_I \le 0.7\,\text{V}$, Q is cut off and $v_O = 5\,\text{V}$. For $v_I > 0.7\,\text{V}$, Q turns on and is biased in the active region, so that

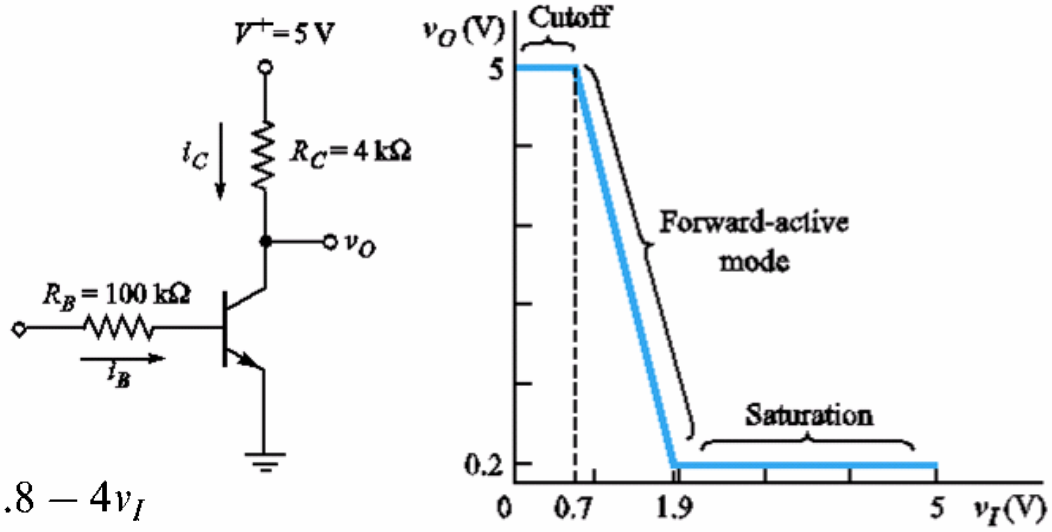
$$i_B = \frac{v_I - V_{BE}(\text{on})}{R_B} = \frac{v_I - 0.7}{100\,\text{k}\Omega}$$

The output voltage is

$$v_O = V^+ - i_C R_C = V^+ - \beta_F i_B R_C$$

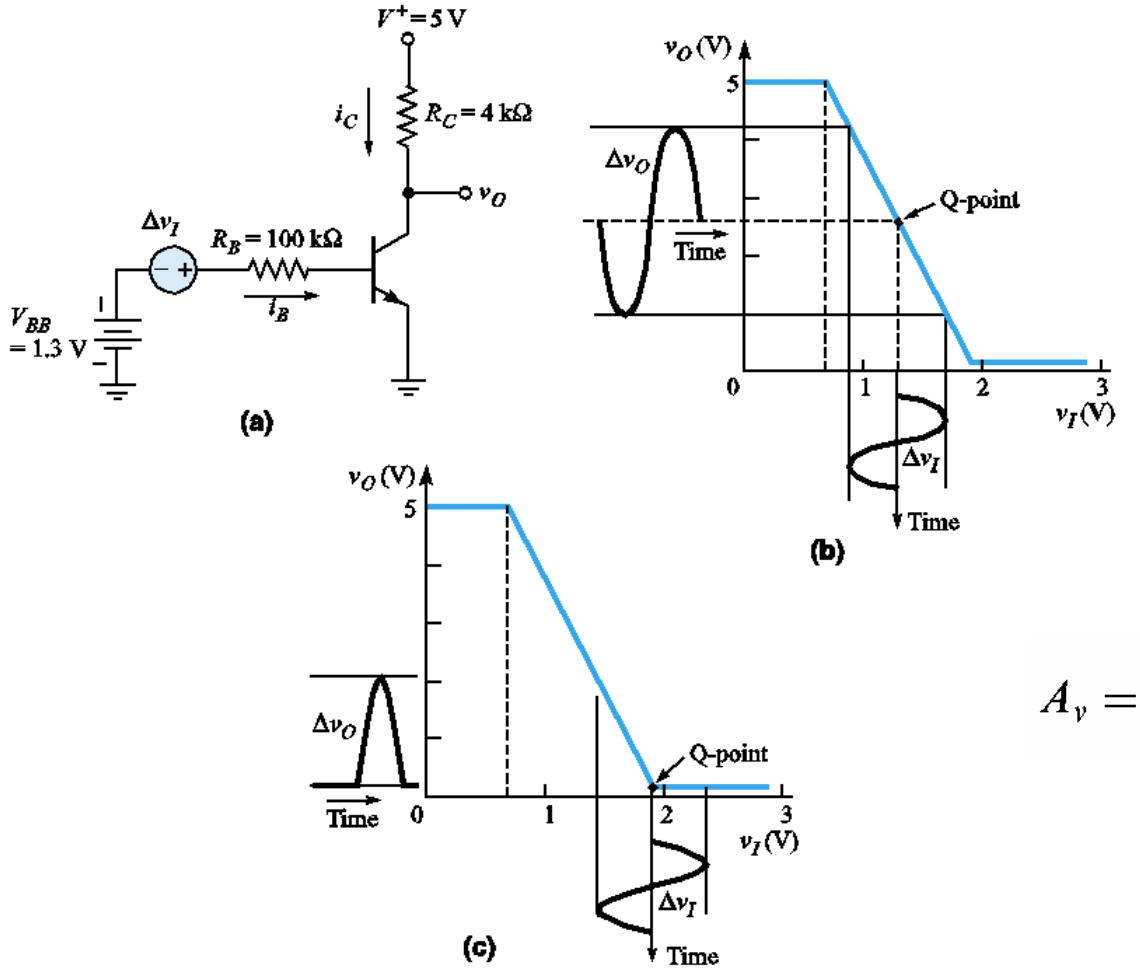
or

$$v_O = 5 - (100)\left[\frac{v_I - 0.7}{100\,k\Omega}\right](4\,k\Omega) = 7.8 - 4v_I$$



This equation is valid for $v_I \ge 0.7\,\text{V}$ and $v_O \ge V_{CE}(\text{sat}) = 0.2\,\text{V}$. The input voltage for $v_O = 0.2\,\text{V}$ is found to be $v_I = 1.9\,\text{V}$. Now, for $v_I > 1.9\,\text{V}$, the transistor is biased in saturation and the output voltage is constant at 0.2 V. The voltage transfer characteristics are shown in Figure 3.44(b).

AC Solution: Now bias the transistor in the center of the active region with an input voltage of $v_I = V_{BB} = 1.3\,\text{V}$. Also include a second input voltage source, denoted as Δv_I in Figure 3.45(a). The dc output voltage is 2.6 V, which is the Q-point of the transistor.



$$A_v = \frac{\Delta v_O}{\Delta v_I} = -4$$

Figure 3.45 (a) The inverter circuit with both a dc and an ac input signal; (b) the dc voltage transfer characteristics, *Q*-point, and sinusoidal input and output signals; (c) the transfer characteristics showing improper dc biasing

Single Base Resistor Biasing

Design Example 3.13 **Objective:** Design the circuit shown in Figure 3.50(b) to yield a given I_{CQ} and V_{CEQ}.

Assume that $V_{CC} = 12\,\text{V}$, $\beta = 100$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$. The Q-point values are to be $I_{CQ} = 1\,\text{mA}$ and $V_{CEQ} = 6\,\text{V}$.

Solution: The collector resistance can be found from

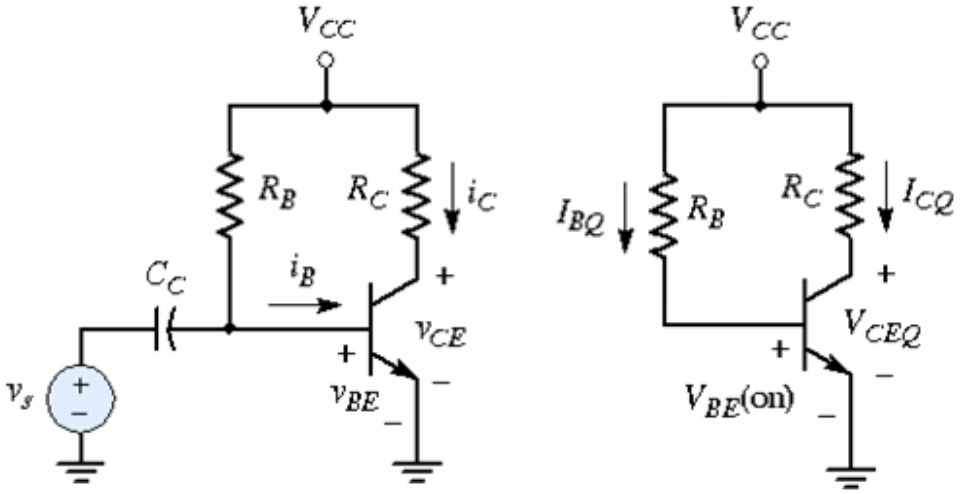
$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{12 - 6}{1} = 6\,\text{k}\Omega$$

The base current must then be

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1\,\text{mA}}{100} \Rightarrow 10\,\mu\text{A}$$

and the base resistance is determined to be

$$R_B = \frac{V_{CC} - V_{BE}(\text{on})}{I_{BQ}} = \frac{12 - 0.7}{10\,\mu\text{A}} = 1.13\,\text{M}\Omega$$



Comment: Although a value of $1.13\,\text{M}\Omega$ for R_B will establish the required base current, this resistance is too large to be used in an integrated circuit.

Q-Point

- Using the same values of the resistances, the shift of Q-point is significant due to the variation of the value of β.

$$I_{BQ} = \frac{V_{CC} - V_{BE}(\text{on})}{R_B} = 10\,\mu\text{A (unchanged)}$$

$$I_{CQ} = \beta I_{BQ} = (50)(10\,\mu\text{A}) \Rightarrow 0.5\,\text{mA}$$

and

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 12 - (0.5)(6) = 9\,\text{V}$$

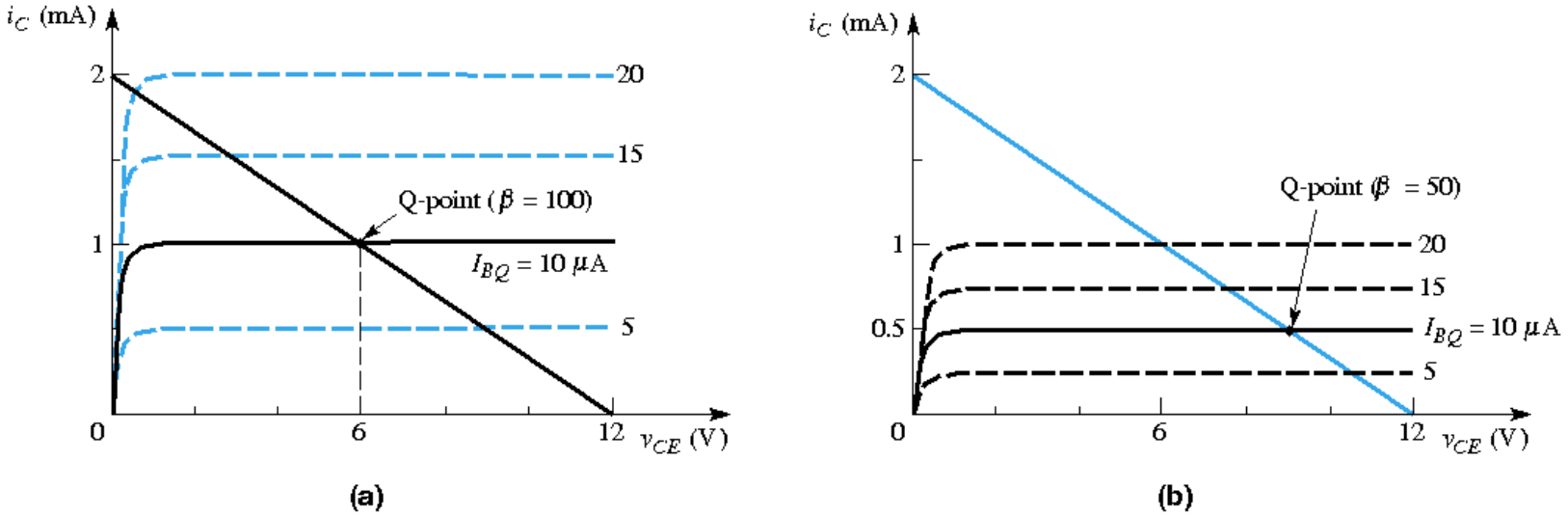


Figure 3.51 Transistor characteristics and load line for the circuit in Example 3.13 when (a) $\beta = 100$ and (b) $\beta = 50$

Voltage Divider Biasing

$$R_{TH} = R_1 // R_2 \qquad V_{TH} = I_{BQ}R_{TH} + V_{BE}(on) + (1+\beta)I_{BQ}R_E$$

$$V_{TH} = \frac{R_2}{R_1 + R_2}V_{CC} \qquad I_{BQ} = \frac{V_{TH} - V_{BE}(on)}{R_{TH} + (1+\beta)R_E}$$

$$I_{CQ} = \beta I_{BQ}$$

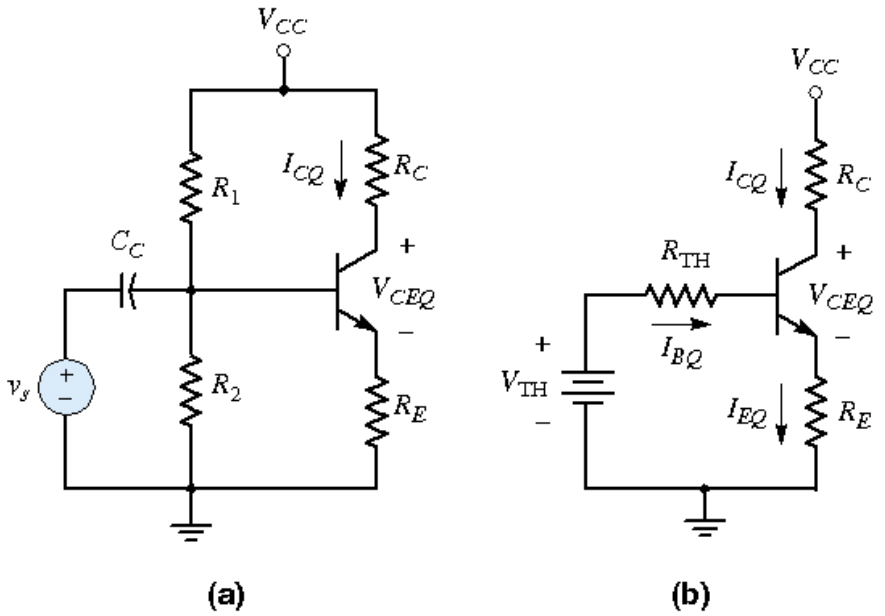


Figure 3.53 (a) A common-emitter circuit with an emitter resistor and voltage divider bias circuit in the base; (b) the dc circuit with a Thevenin equivalent base circuit

Example 3.14 **Objective:** Analyze a circuit using a voltage divider bias circuit, and determine the change in the Q-point with a variation in β when the circuit contains an emitter resistor.

For the circuit given in Figure 3.53(a), let $R_1 = 56\,\text{k}\Omega$, $R_2 = 12.2\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $R_E = 0.4\,\text{k}\Omega$, $V_{CC} = 10\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 100$.

Solution: Using the Thevenin equivalent circuit in Figure 3.53(b), we have

$$R_{TH} = R_1 \| R_2 = 56 \| 12.2 = 10.0\,\text{k}\Omega$$

and

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right) \cdot V_{CC} = \left(\frac{12.2}{56 + 12.2}\right)(10) = 1.79\,\text{V}$$

Writing the Kirchhoff voltage law equation around the B–E loop, we obtain

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1+\beta)R_E} = \frac{1.79 - 0.7}{10 + (101)(0.4)} \Rightarrow 21.6\,\mu\text{A}$$

The collector current is

$$I_{CQ} = \beta I_{BQ} = (100)(21.6\,\mu\text{A}) \Rightarrow 2.16\,\text{mA}$$

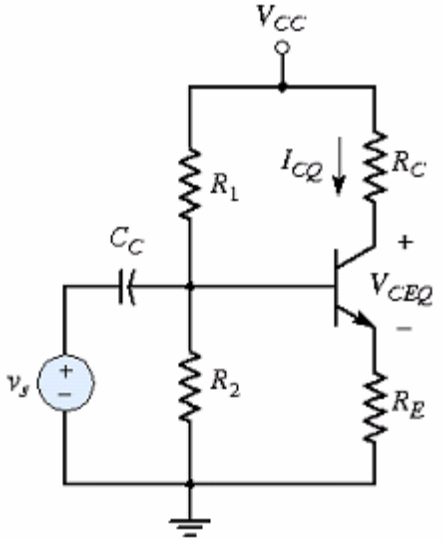
and the emitter current is

$$I_{EQ} = (1+\beta)I_{BQ} = (101)(21.6\,\mu\text{A}) \Rightarrow 2.18\,\text{mA}$$

The quiescent C–E voltage is then

$$V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E = 10 - (2.16)(2) - (2.18)(0.4) = 4.81\,\text{V}$$

These results show that the transistor is biased in the active region.



If the current gain of the transistor were to decrease to $\beta_F = 50$ or increase to $\beta_F = 150$, we obtain the following results:

β_F	I_{BQ}(μA)	I_{CQ}(mA)	I_{EQ}(mA)	V_{CEQ}(V)
50	35.9	1.80	1.83	5.67
100	21.6	2.16	2.18	4.81
150	15.5	2.32	2.34	4.40

For a 3 : 1 ratio in β_F, the collector current and collector-emitter voltage change by only a 1.29 : 1 ratio.

Comment: The voltage divider circuit of R_1 and R_2 can bias the transistor in its active region using resistor values in the low kilohm range. In contrast, single resistor biasing requires a resistor in the megohm range. In addition, the change in I_{CQ} and V_{CEQ} with a change in β_F has been substantially reduced compared to the change shown in Figure 3.51. Including an emitter resistor R_E has tended to **stabilize** the Q-point. This means that including the emitter resistor helps to stabilize the Q-point with respect to variations in β.

Bias Stability

The design requirement for bias stability is $R_{TH} \ll (1+\beta)R_E$. Consequently, the collector current, from Equation (3.38), becomes approximately

$$I_{CQ} \cong \frac{\beta(V_{TH} - V_{BE}(\text{on}))}{(1+\beta)R_E}$$

Normally, $\beta \gg 1$; therefore, $\beta/(1+\beta) \cong 1$, and

$$I_{CQ} \cong \frac{(V_{TH} - V_{BE}(\text{on}))}{R_E}$$

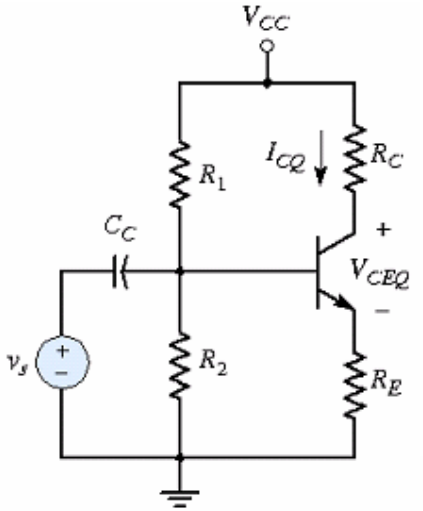
Now the quiescent collector current is essentially a function of only the dc voltages and the emitter resistance, and the Q-point is stabilized against β variations. However, if R_{TH} is too small, then R_1 and R_2 are small, and excessive power is dissipated in these resistors. The general rule is that a circuit is considered **bias stable** when

$$R_{TH} \cong 0.1(1+\beta)R_E$$

Design Example 3.15 **Objective:** Design a bias-stable circuit.

Consider the circuit shown in Figure 3.53(a). Let $V_{CC} = 5\,\text{V}$, $R_C = 1\,\text{k}\Omega$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 120$. Choose R_E and determine R_1 and R_2 such that the circuit is bias stable and that $V_{CEQ} = 3\,\text{V}$.

Design Pointer: Typically, the voltage across R_E should be on the same order of magnitude as $V_{BE}(\text{on})$. Larger voltage drops may mean the supply voltage V_{CC} has to be increased in order to get the required voltage across the collector-emitter and across R_C.



Solution: With $\beta = 120$, $I_{CQ} \approx I_{EQ}$. Then, choosing a standard value of 0.51 kΩ for R_E, we find

$$I_{CQ} \cong \frac{V_{CC} - V_{CEQ}}{R_C + R_E} = \frac{5-3}{1+0.51} = 1.32\,\text{mA}$$

The voltage drop across R_E is now $(1.32)(0.51) = 0.673\,\text{V}$, which is approximately the desired value. The base current is found to be

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.32}{120} \Rightarrow 11.0\,\mu\text{A}$$

Using the Thevenin equivalent circuit in Figure 3.53(b), we find

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1+\beta)R_E}$$

For a bias-stable circuit, $R_{TH} = 0.1(1+\beta)R_E$, or

$$R_{TH} = (0.1)(121)(0.51) = 6.17\,\text{k}\Omega$$

Then,

$$I_{BQ} = 11.0\,\mu\text{A} \Rightarrow \frac{V_{TH} - 0.7}{6.17 + (121)(0.51)}$$

which yields

$$V_{TH} = 0.747 + 0.70 = 1.45\,\text{V}$$

Now

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{R_2}{R_1 + R_2}\right)5 = 1.45\,\text{V}$$

or

$$\left(\frac{R_2}{R_1 + R_2}\right) = \frac{1.45}{5} = 0.288$$

Also,

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = 6.05\,\text{k}\Omega = R_1\left(\frac{R_2}{R_1 + R_2}\right) = R_1(0.288)$$

which yields

$$R_1 = 21\,\text{k}\Omega$$

and

$$R_2 = 8.5\,\text{k}\Omega$$

From Appendix D, we can choose standard resistor values of $R_1 = 20\,\text{k}\Omega$ and $R_2 = 8.2\,\text{k}\Omega$.

Positive and Negative Voltage Biasing

EXAMPLE 5.18

Objective: Consider the analysis of a transistor circuit with an npn transistor biased with both positive and negative dc voltages. Consider the circuit shown in Figure 5.61 in which the signal source is connected directly to the base of the transistor.

Solution: For the dc analysis, we set $v_s = 0$ so that the base terminal is at ground potential. We assume transistor parameters of $\beta = 100$ and $V_{BE}(\text{on}) = 0.7$ V.

The KVL equation around the B–E loop is

$$0 = V_{BE}(\text{on}) + I_{EQ}R_E + V^-$$

or

$$I_{EQ} = \frac{-(V^- + V_{BE}(\text{on}))}{R_E} = \frac{-(-5 + 0.7)}{2} = 2.15\,\text{mA}$$

Now

$$I_{CQ} = \left(\frac{\beta}{1+\beta}\right) \cdot I_{EQ} = \left(\frac{100}{101}\right)(2.15) = 2.13\,\text{mA}$$

A KVL equation around the collector–emitter loop yields

$$V^+ = I_{CQ}R_C + V_{CEQ} + I_{EQ}R_E + V^-$$

or

$$V_{CEQ} = (V^+ - V^-) - I_{CQ}R_C - I_{EQ}R_E$$
$$= (5 + 5) - (2.13)(1.5) - (2.15)(2)$$

or

$$V_{CEQ} = 2.51\,\text{V}$$

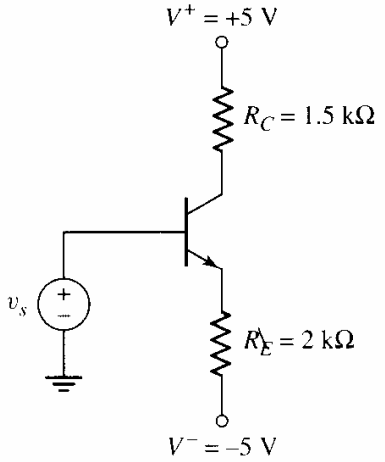


Figure 5.61 Simple transistor circuit biased with both positive and negative dc voltages

EXAMPLE 5.19

Objective: Design a bias-stable pnp transistor circuit to meet a set of specifications.

Specifications: The circuit configuration to be designed is shown in Figure 5.63(a). The transistor Q-point values are to be: $V_{ECQ} = 7$ V, $I_{CQ} \cong 0.5$ mA, and $V_{RE} \cong 1$ V. Assume transistor parameters of $\beta = 80$ and $V_{EB}(\text{on}) = 0.7$ V.

Choices: Assume transistor parameters of $\beta = 80$ and $V_{EB}(\text{on}) = 0.7$ V. Standard resistor values are to be used in the final design.

Solution: The Thevenin equivalent circuit is shown in Figure 5.63(b). The Thevenin equivalent resistance is $R_{TH} = R_1 \| R_2$ and the Thevenin equivalent voltage, measured with respect to ground, is given by

$$V_{TH} = \left(\frac{R_2}{R_1 + R_R}\right)(V^+ - V^-) + V^-$$

$$= \frac{1}{R_1}\left(\frac{R_1 R_2}{R_1 + R_2}\right)(V^+ - V^-) + V^-$$

For $V_{RE} \cong 1$ V and $I_{CQ} \cong 0.5$ mA, then we can set

$$R_E = \frac{1}{0.5} = 2\,\text{k}\Omega$$

For a bias stable circuit, we want

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = (0.1)(1 + \beta)R_E$$

$$= (0.1)(81)(2) = 16.2\,\text{k}\Omega$$

Then the Thevenin equivalent voltage can be written as

$$V_{TH} = \frac{1}{R_1}(16.2)[9 - (-9)] + (-9) = \frac{1}{R_1}(291.6) - 9$$

The KVL equation around the E–B loop is given by

$$V^+ = I_{EQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_{TH} + V_{TH}$$

The transistor is to be biased in the forward-active mode so that $I_{EQ} = (1 + \beta)I_{BQ}$. We then have

$$V^+ = (1 + \beta)I_{BQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_{TH} + V_{TH}$$

For $I_{CQ} = 0.5$ mA, then $I_{BQ} = 0.00625$ mA so we can write

$$9 = (81)(0.00625)(2) + 0.7 + (0.00625)(16.2) + \frac{1}{R_1}(291.6) - 9$$

We find $R_1 = 18.0\,\text{k}\Omega$. Then, from $R_{TH} = R_1 \| R_2 = 16.2\,\text{k}\Omega$, we find $R_2 = 162\,\text{k}\Omega$.

For $I_{CQ} = 0.5$ mA, then $I_{EQ} = 0.506$ mA. The KVL equation around the E–C loop yields

$$V^+ = I_{EQ}R_E + V_{ECQ} + I_{CQ}R_C + V^-$$

or

$$9 = (0.506)(2) + 7 + (0.50)R_C + (-9)$$

which yields

$$R_C \cong 20\,\text{k}\Omega$$

Integrated Circuit Biasing

- For integrated circuits, we would like to eliminate as many resistors as possible since, in general, they require a larger surface than transistors.

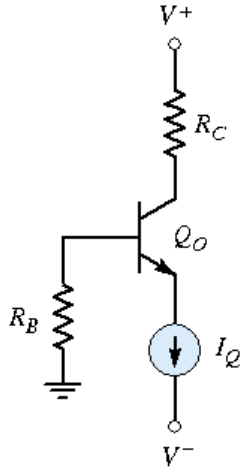


Figure 3.56 Bipolar transistor biased with a constant-current source

$$0 = I_1 R_1 + V_{BE}(on) + V^-$$

$$I_1 = \frac{-(V_{BE}(on) + V^-)}{R_1}$$ Reference current

$$I_1 = I_{C1} + I_{B1} + I_{B2} = I_{C1} + 2I_{B2}$$

$$= I_{C2} + \frac{2I_{C2}}{\beta} = (1 + \frac{2}{\beta})I_{C2}$$

$$I_{C2} = I_1 \Big/ (1 + \frac{2}{\beta}) \approx I_1$$

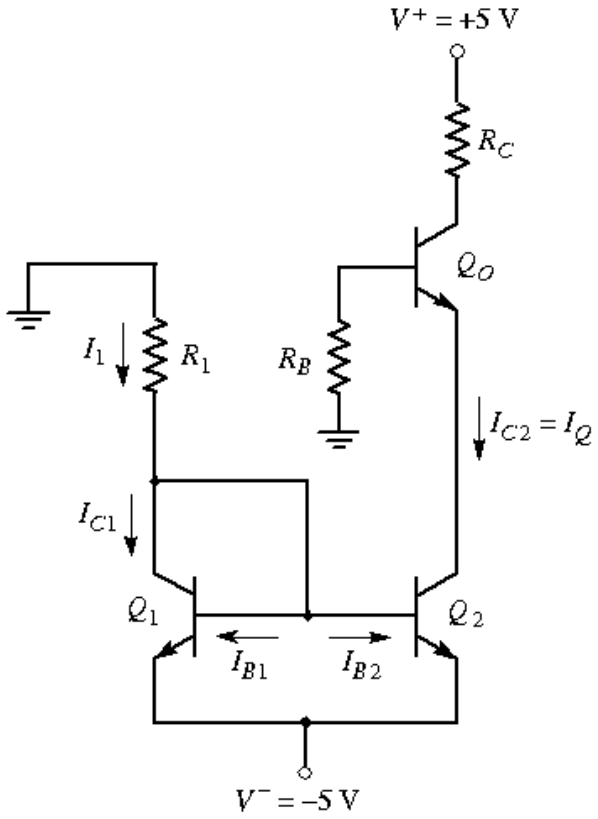


Figure 3.57 Constant-current source biasing

Example 3.16 **Objective:** Determine the currents in a two-transistor current source.

For the circuit in Figure 3.57, the circuit and transistor parameters are: $R_1 = 10\,\text{k}\Omega$, $\beta = 50$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$.

Solution: The reference current is

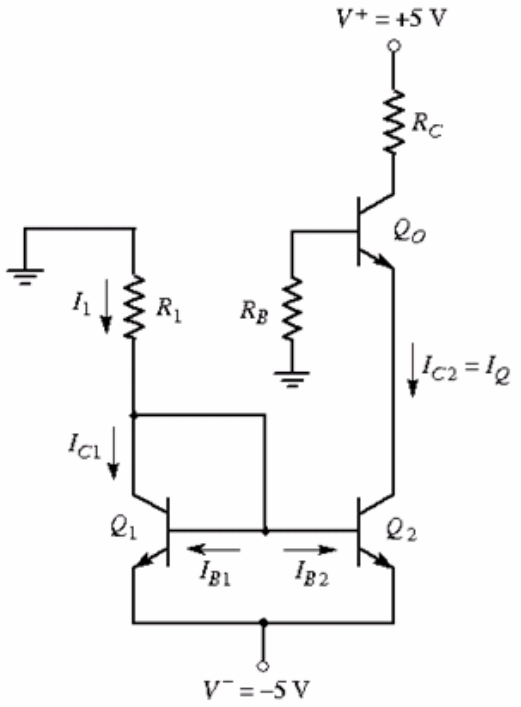
$$I_1 = \frac{-(V^- + V_{BE}(\text{on}))}{R_1} = \frac{-((-5) + 0.7)}{10} = 0.43\,\text{mA}$$

From Equation (3.45), the bias current I_Q is

$$I_{C2} = I_Q = \frac{I_1}{\left(1 + \frac{2}{\beta}\right)} = \frac{0.43}{\left(1 + \frac{2}{50}\right)} = 0.413\,\text{mA}$$

The base currents are then

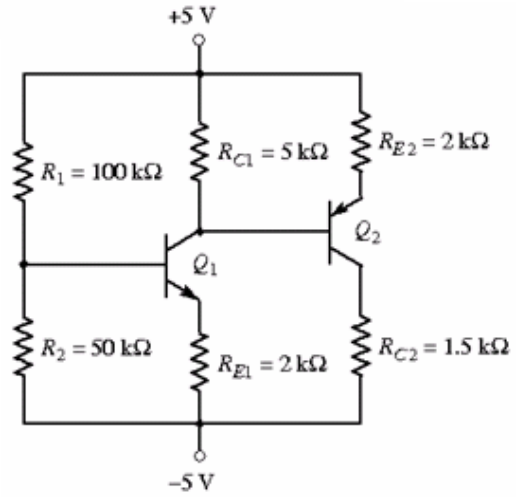
$$I_{B1} = I_{B2} = \frac{I_{C2}}{\beta} = \frac{0.413}{50} \Rightarrow 8.26\,\mu\text{A}$$



Comment: For relatively large values of current gain β, the bias current I_Q is essentially the same as the reference current I_1.

Example 3.17 **Objective:** Calculate the dc voltages at each node and the dc currents through the elements in a multistage circuit.

For the circuit in Figure 3.59, assume the B–E turn-on voltage is 0.7 V and $\beta = 100$ for each transistor.



$$R_{TH} = R_1 \| R_2 = 100 \| 50 = 33.3\,\text{k}\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5 = \left(\frac{50}{150}\right)(10) - 5 = -1.67\,\text{V}$$

$$V_{TH} = I_{B1} R_{TH} + V_{BE}(\text{on}) + I_{E1} R_{E1} - 5$$

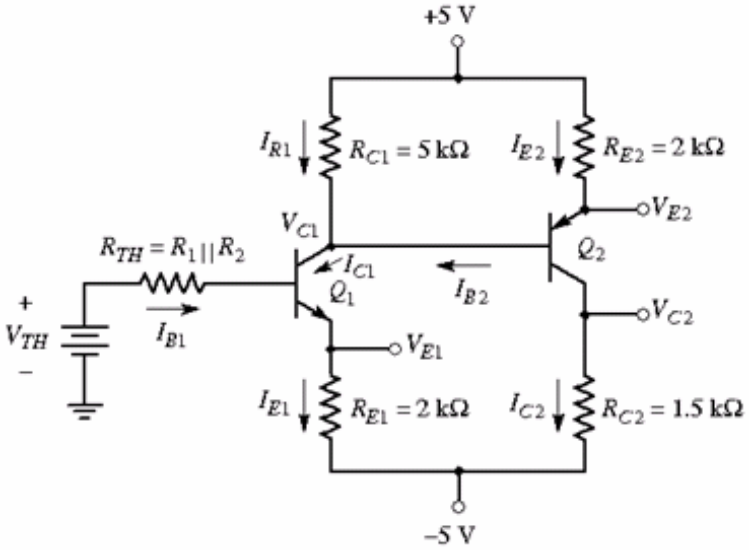
$$I_{B1} = \frac{-1.67 + 5 - 0.7}{33.3 + (101)(2)} \Rightarrow 11.2\,\mu\text{A}$$

$$I_{C1} = 1.12\,\text{mA}$$

$$I_{R1} + I_{B2} = I_{C1}$$

$$\frac{5 - V_{C1}}{R_{C1}} + I_{B2} = I_{C1} \Rightarrow \frac{5 - \mathbf{V_{C1}}}{5} + \mathbf{I_{B2}} = \mathbf{1.12}$$

$$I_{B2} = \frac{I_{E2}}{1+\beta} = \frac{5 - V_{E2}}{(1+\beta)R_{E2}} = \frac{5 - (V_{C1} + 0.7)}{(1+\beta)R_{E2}} \Rightarrow \mathbf{I_{B2}} = \frac{\mathbf{5 - V_{C1} - 0.7}}{\mathbf{101 \times 2}}$$



$$\Rightarrow \mathbf{I_{B2} = 0.0237mA,\ I_{E2} = 2.39mA}$$

$$\mathbf{V_{C1} = -0.48V,\ V_{E2} = 5 - 2 \times 2.39 = 0.22V}$$

$$\mathbf{V_{C2} = -5 + 1.5 \times 2.37 = -1.445V}$$

EXAMPLE 5.22

Objective: Design the circuit shown in Figure 5.69, called a cascode circuit, to meet the following specifications: $V_{CE1} = V_{CE2} = 2.5$ V, $V_{RE} = 0.7$ V, $I_{C1} \cong I_{C2} \cong 1$ mA, and $I_{R1} \cong I_{R2} \cong I_{R3} \cong 0.10$ mA.

Solution: The initial design will neglect base currents. We can then define $I_{\text{Bias}} = I_{R1} = I_{R2} = I_{R3} = 0.10$ mA. Then

$$R_1 + R_2 + R_3 = \frac{V^+}{I_{\text{Bias}}} = \frac{9}{0.10} = 90\,\text{k}\Omega$$

The voltage at the base of Q_1 is

$$V_{B1} = V_{RE} + V_{BE}(\text{on}) = 0.7 + 0.7 = 1.4\,\text{V}$$

Then

$$R_3 = \frac{V_{B1}}{I_{\text{Bias}}} = \frac{1.4}{0.10} = 14\,\text{k}\Omega$$

The voltage at the base of Q_2 is

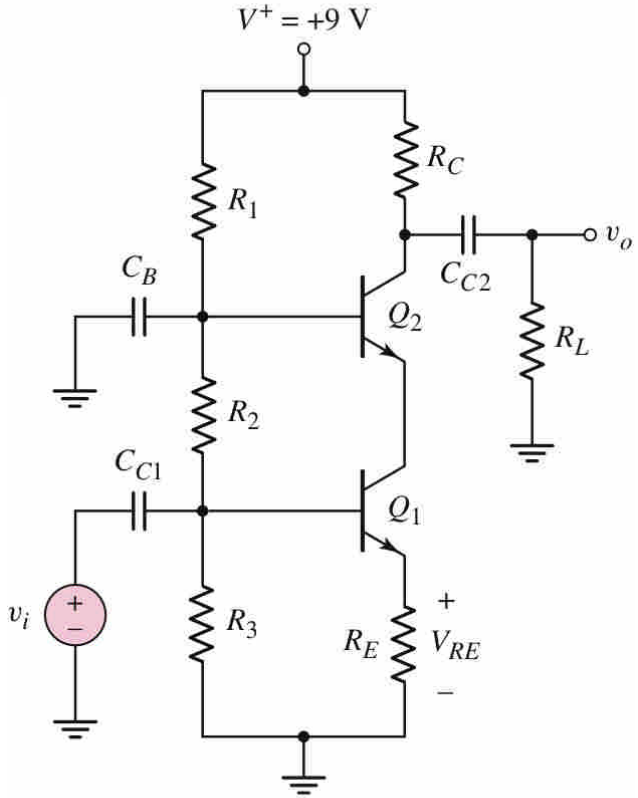
$$V_{B2} = V_{RE} + V_{CE1} + V_{BE}(\text{on}) = 0.7 + 2.5 + 0.7 = 3.9\,\text{V}$$

Then

$$R_2 = \frac{V_{B2} - V_{B1}}{I_{\text{Bias}}} = \frac{3.9 - 1.4}{0.10} = 25\,\text{k}\Omega$$

We then obtain

$$R_1 = 90 - 25 - 14 = 51\,\text{k}\Omega$$



The emitter resistor R_E can be found as

$$R_E = \frac{V_{RE}}{I_{C1}} = \frac{0.7}{1} = 0.7\,\text{k}\Omega$$

The voltage at the collector of Q_2 is

$$V_{C2} = V_{RE} + V_{CE1} + V_{CE2} = 0.7 + 2.5 + 2.5 = 5.7\,\text{V}$$

Then

$$R_C = \frac{V^+ - V_{C2}}{I_{C2}} = \frac{9 - 5.7}{1} = 3.3\,\text{k}\Omega$$

Comment: By neglecting base currents, the design of this circuit is straightf
A computer analysis using PSpice, for example, will verify the design or sh
small changes need to be made to meet the design specifications.

We will see the cascode circuit again in Section 6.9.3 of the next chapter.

One advantage of the cascode circuit will be determined in Chapter 7.
code circuit has a larger bandwidth than just a simple common-emitter ampli