Basic BJT Amplifiers

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The Bipolar Linear Amplifier

- To use the circuit as an amplifier, the transistor needs to be biased with a dc voltage at a quiescent point (Q-point), such that the transistor is biased in the forward-active region.
- If the transistor is not biased in the active region, the output voltage does not change with a change in the input voltage.

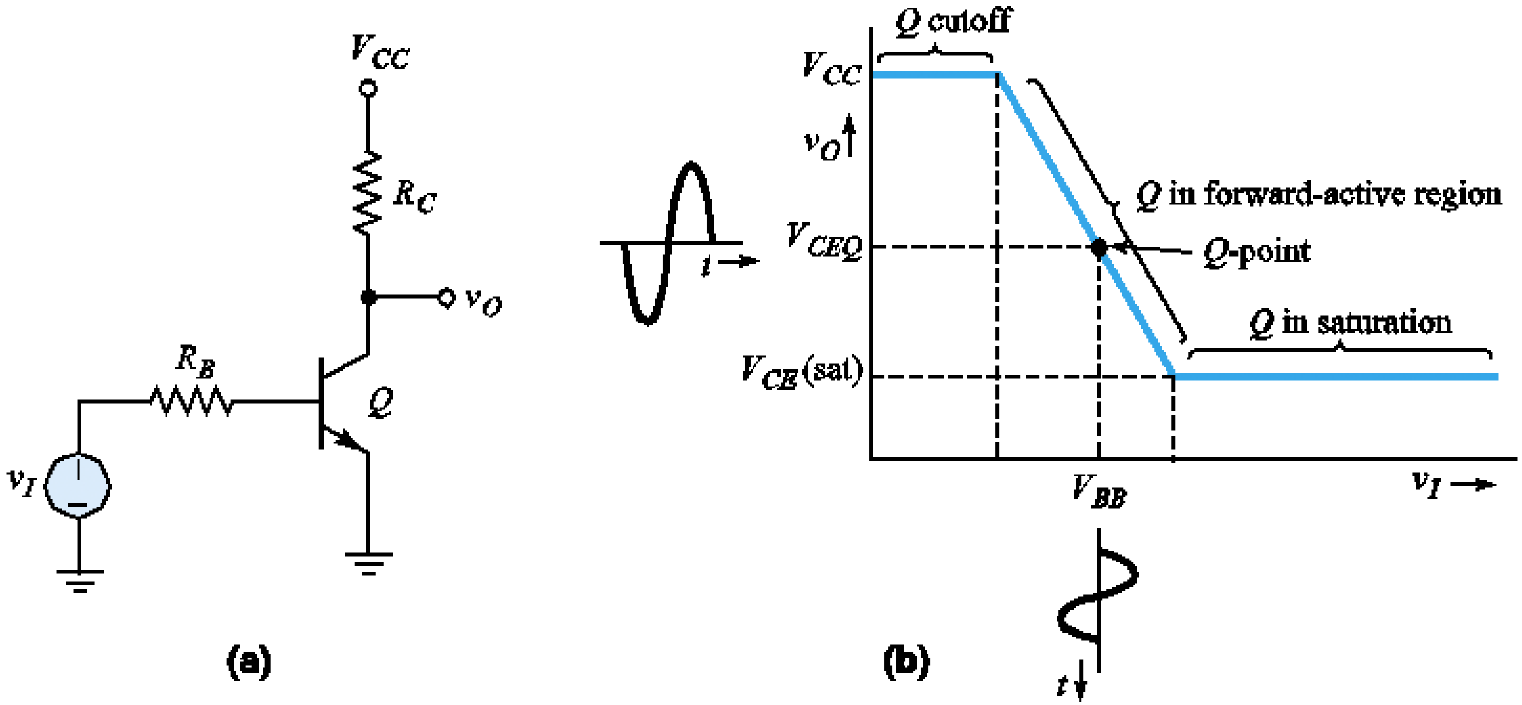


Figure 4.2 (a) Bipolar transistor inverter circuit; (b) inverter transfer characteristics

The Bipolar Linear Amplifier

- To obtain a linear amplifier, the time-varying or ac currents and voltages must be small enough to ensure a linear relation between the ac signals.

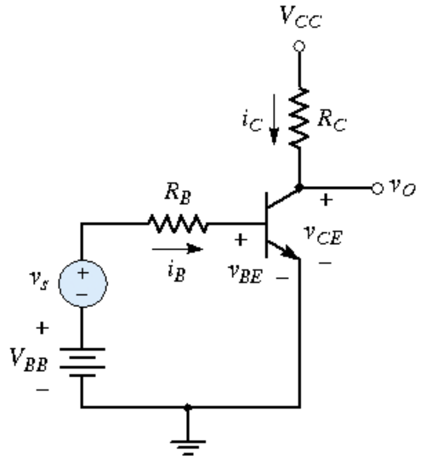


Figure 4.3 A common-emitter circuit with time-varying signal source in series with the base dc source

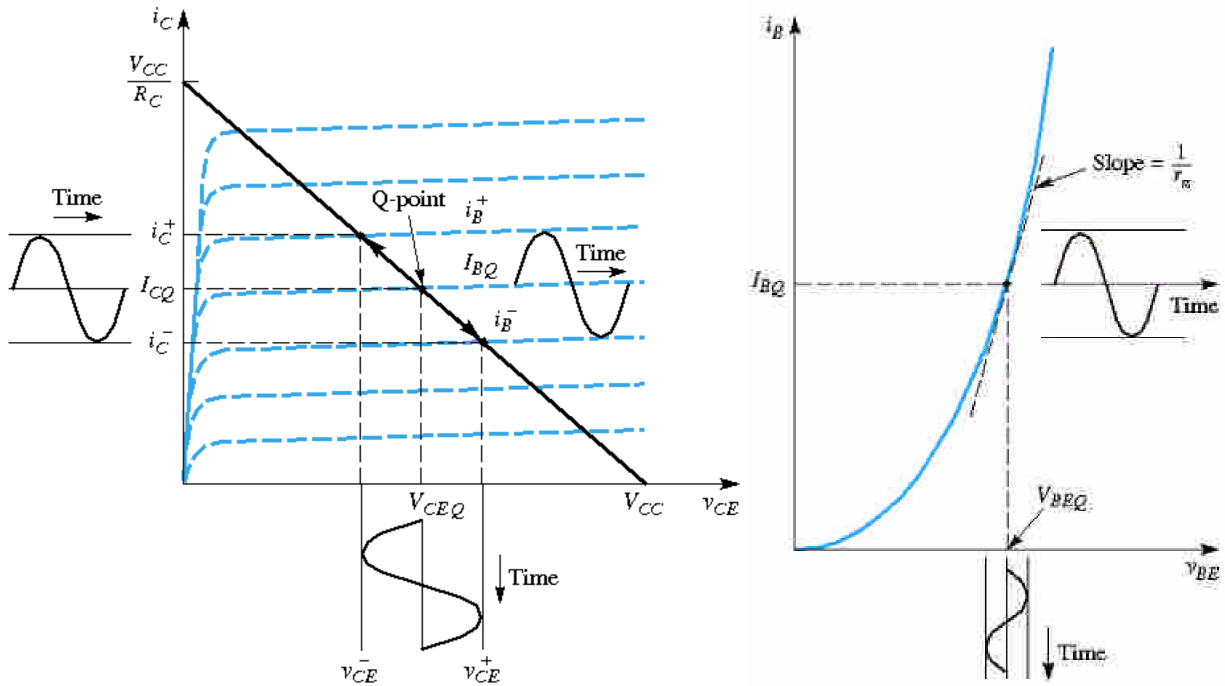


Figure 4.4 Common-emitter transistor characteristics, dc load line, and sinusoidal variation in base current, collector current, and collector–emitter voltage

Analysis of AC Circuit (Small Signal Analysis)

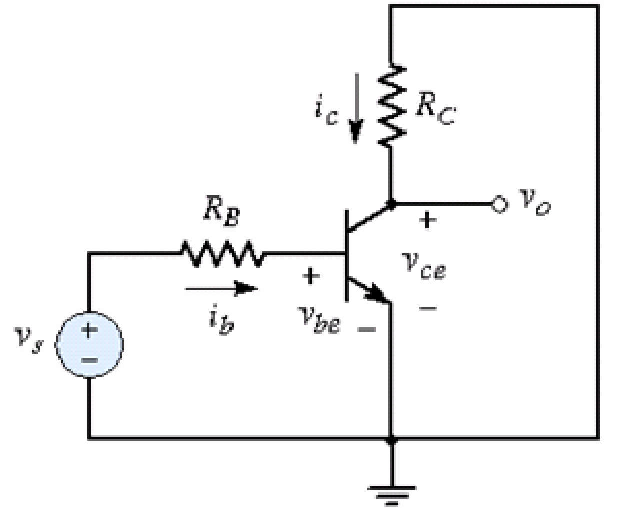
- Assume that the transistor is baised in the forward-active region with appropriate dc voltages and currents.

BE is forward-biased, $i_E = I_S \exp(v_{BE}/V_T)$

$$i_B = \frac{I_S}{1+\beta}\exp(v_{BE}/V_T) = \frac{I_S}{1+\beta}\exp((V_{BEQ}+v_{be})/V_T) = \frac{I_S}{1+\beta}\exp(V_{BEQ}/V_T)\exp(v_{be}/V_T)$$

$$= I_{BQ}\exp(v_{be}/V_T) \approx I_{BQ}(1+v_{be}/V_T) = I_{BQ} + i_b$$

$$i_b = (I_{BQ}/V_T)v_{be}$$



Similarly, we have:

$$\begin{cases} i_B = I_{BQ} + i_b \\ i_C = I_{CQ} + i_c \\ v_{CE} = V_{CEQ} + v_{ce} \\ v_{BE} = V_{BEQ} + v_{be} \end{cases}$$

DC Components:

$$V_{BB} = I_{BQ}R_B + V_{BEQ}$$
$$V_{CC} = I_{CQ}R_C + V_{CEQ}$$

DC+AC Components:

$$V_{BB} + v_s = i_B R_B + v_{BE} = (I_{BQ} + i_b)R_B + (V_{BEQ} + v_{be})$$
$$V_{CC} = i_C R_C + v_{CE} = (I_{CQ} + i_c)R_C + (V_{CEQ} + v_{ce})$$

AC Components:

$$v_s = i_b R_B + v_{be}$$
$$i_c R_C + v_{ce} = 0$$

Small Signal Hybrid-π Equivalent Circuit

$$v_{be} = i_b r_\pi$$

$$\frac{1}{r_\pi} = \left.\frac{\partial i_B}{\partial v_{BE}}\right|_Q = \frac{\partial}{\partial v_{BE}}\left[\frac{I_S}{1+\beta}\exp(v_{BE}/V_T)\right]\Bigg|_Q$$

$$= \frac{1}{V_T}\left[\frac{I_S}{1+\beta}\exp(v_{BE}/V_T)\right]\Bigg|_Q = \frac{I_{BQ}}{V_T}$$

r_π : diffusion resistance

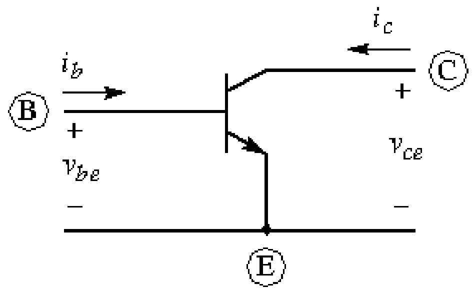


Figure 4.7 The BJT as a small-signal, two-port network

$$i_C = \alpha I_S \exp(v_{BE}/V_T)$$

$$\frac{\Delta i_C}{\Delta v_{BE}} = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_Q = \frac{1}{V_T}\alpha I_S \exp(v_{BE}/V_T) = \frac{I_{CQ}}{V_T} = g_m$$

g_m : transconductance

$$\boxed{r_\pi g_m = \frac{V_T}{I_{BQ}} \cdot \frac{I_{CQ}}{V_T} = \beta}$$

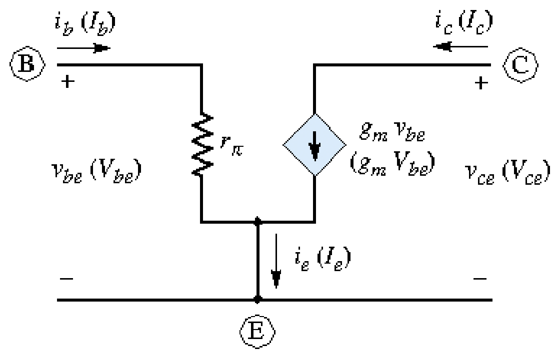


Figure 4.8 A simplified small-signal hybrid-π equivalent circuit for the npn transistor

Small Signal Hybrid-π Equivalent Circuit

$$\Delta i_C = \left.\frac{\partial i_C}{\partial i_B}\right|_Q \cdot \Delta i_B$$

$$\therefore \frac{i_c}{i_b} = \left.\frac{\partial i_C}{\partial i_B}\right|_Q = \beta$$

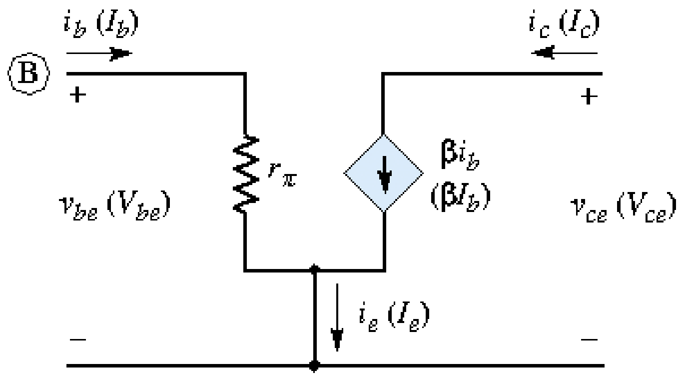


Figure 4.9 BJT small-signal equivalent circuit using common-emitter current gain

Small Signal Hybrid-π Equivalent Circuit

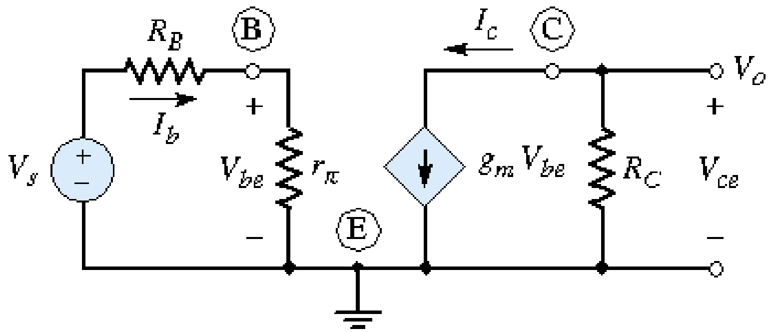


Figure 4.11 The small-signal equivalent circuit of the common-emitter circuit using the npn transistor hybrid-π model

$$V_o = -g_m V_{be} R_C$$

$$V_{be} = \left(\frac{r_\pi}{r_\pi + R_B}\right) V_s$$

$$A_v = \frac{V_o}{V_s} = -g_m R_C \frac{r_\pi}{r_\pi + R_B}$$

$$V_o = -\beta I_b R_C$$

$$I_b = \frac{V_s}{r_\pi + R_B}$$

$$A_v = \frac{V_o}{V_s} = -\frac{\beta R_C}{r_\pi + R_B}$$

Example 4.1 **Objective:** Calculate the small-signal voltage gain of the bipolar transistor circuit shown in Figure 4.3.

Assume the transistor and circuit parameters are: $\beta = 100$, $V_{CC} = 12\,\text{V}$, $V_{BE} = 0.7\,\text{V}$, $R_C = 6\,\text{k}\Omega$, $R_B = 50\,\text{k}\Omega$, and $V_{BB} = 1.2\,\text{V}$.

DC Solution: We first do the dc analysis to find the Q-point values. We obtain

$$I_{BQ} = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{1.2 - 0.7}{50} \Rightarrow 10\,\mu\text{A}$$

so that

$$I_{CQ} = \beta I_{BQ} = (100)(10\,\mu\text{A}) \Rightarrow 1\,\text{mA}$$

Then,

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 12 - (1)(6) = 6\,\text{V}$$

Therefore, the transistor is biased in the forward-active mode.

AC Solution: The small-signal hybrid-π parameters are

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{1} = 2.6\,\text{k}\Omega$$

and

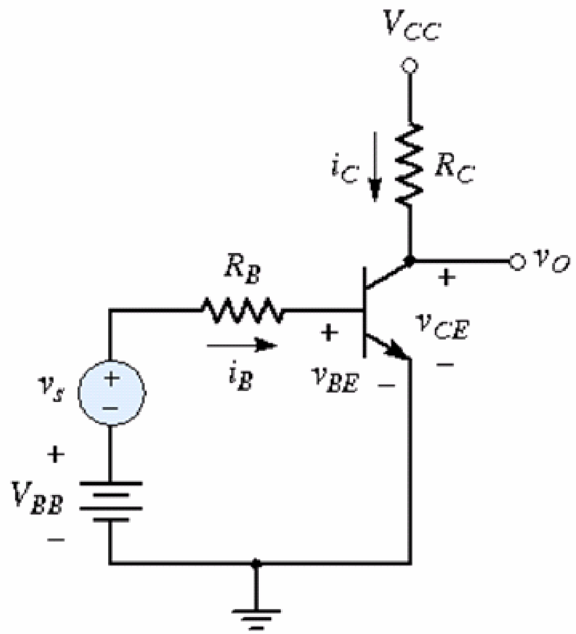
$$g_m = \frac{I_{CQ}}{V_T} = \frac{1}{0.026} = 38.5\,\text{mA/V}$$

The small-signal voltage gain is determined using the small-signal equivalent circuit shown in Figure 4.11. From Equation (4.23), we find

$$A_v = \frac{V_o}{V_s} = -(g_m R_C) \cdot \left(\frac{r_\pi}{r_\pi + R_B}\right)$$

or

$$= -(38.5)(6)\left(\frac{2.6}{2.6 + 50}\right) = -11.4$$



DC and AC Circuit Model

Table 4.2 Transformation of elements in dc and small-signal analysis

Element	I–V relationship	DC model	AC model
Resistor	$I_R = \frac{V}{R}$	R	R
Capacitor	$I_C = sCV$	Open	C
Inductor	$I_L = \frac{V}{sL}$	Short	L
Diode	$I_D = I_S(e^{v_D/V_T} - 1)$	$+V_\gamma - r_f$	$r_d = V_T/I_D$
Independent voltage source	$V_S = \text{constant}$	$+\ V_S\ -$	Short
Independent current source	$I_S = \text{constant}$	I_S	Open

Table suggested by Richard Hester of Iowa State University.

Bipolar AC Analysis

Problem-Solving Technique: Bipolar AC Analysis

Since we are dealing with linear amplifier circuits, superposition applies, which means that we can perform the dc and ac analyses separately. The analysis of the BJT amplifier proceeds as follows:

1. Analyze the circuit with only the dc sources present. This solution is the dc or quiescent solution, which uses the dc signal models for the elements, as listed in Table 4.2. The transistor must be biased in the forward-active region in order to produce a linear amplifier.
2. Replace each element in the circuit with its small-signal model, as shown in Table 4.2. The small-signal hybrid-π model applies to the transistor although it is not specifically listed in the table.
3. Analyze the small-signal equivalent circuit, setting the dc source components equal to zero, to produce the response of the circuit to the time-varying input signals only.

Small Signal Equivalent Circuit Including Early Effect

$$i_C = \alpha I_S \exp(v_{BE}/V_T)(1 + v_{CE}/V_T)$$

V_A : is the Early voltage

The output resistance is

$$r_o = \left. \frac{\partial v_{CE}}{\partial i_C} \right|_Q \qquad \frac{1}{r_o} = \left. \frac{\partial i_C}{\partial v_{CE}} \right|_Q = \alpha I_S \exp(v_{BE}/V_T) \cdot \frac{1}{V_A} \approx \frac{I_{CQ}}{V_A}$$

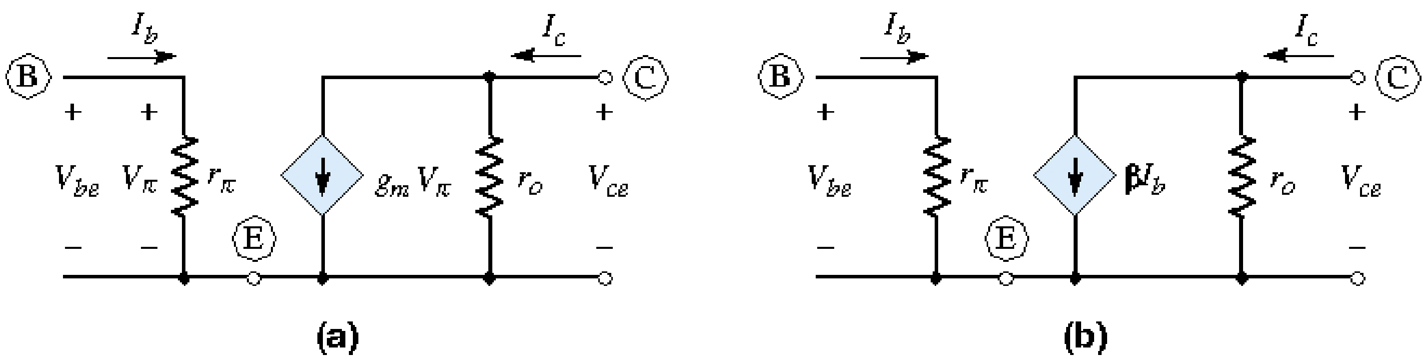


Figure 4.13 Expanded small-signal model of the BJT, including the Early effect, for the case when the circuit contains the (a) transconductance and (b) the current gain parameters

Example 4.2 **Objective:** Determine the small-signal voltage gain, including the effect of the transistor output resistance r_o.

Reconsider the circuit shown in Figure 4.1, with the parameters given in Example 4.1. In addition, assume the Early voltage is $V_A = 50\,\text{V}$.

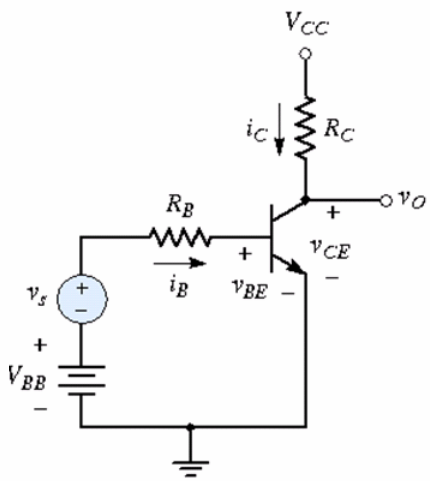
Solution: The small-signal output resistance r_o is determined to be

$$r_o = \frac{V_A}{I_{CQ}} = \frac{50}{1\,\text{mA}} = 50\,\text{k}\Omega$$

Using the small-signal equvialent circuit in Figure 4.11, we see that the output resistance r_o is in parallel with R_C. The small-signal voltage gain is therefore

$$A_v = \frac{V_o}{V_s} = -g_m(R_C \| r_o)\left(\frac{r_\pi}{r_\pi + R_B}\right)$$

$$= -(38.5)(6\|50)\left(\frac{2.6}{2.6+50}\right) = -10.2$$



Comment: Comparing this result to that of Example 4.1, we see that r_o reduces the magnitude of the small-signal voltage gain. In many cases, the magnitude of r_o is much larger than that of R_C, which means that the effect of r_o is negligible.

Small Signal Hybrid-π Equivalent Circuit for PNP BJT

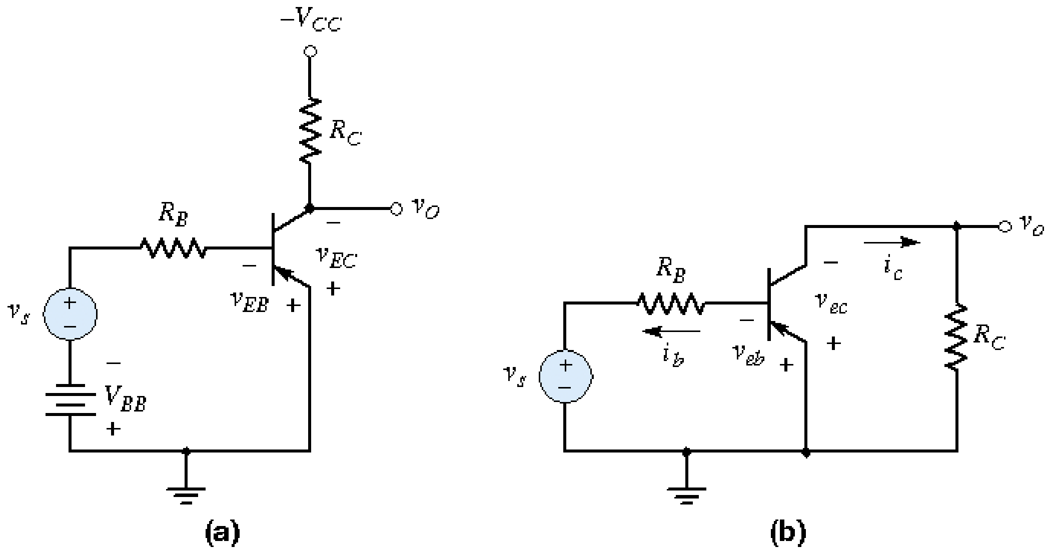


Figure 4.14 (a) A common-emitter circuit with a pnp transistor and (b) the corresponding ac equivalent circuit

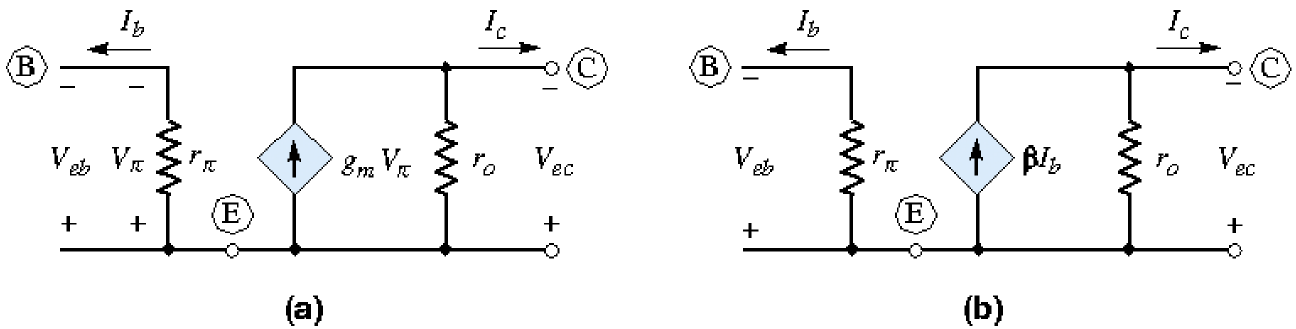


Figure 4.15 The hybrid-π model of the pnp transistor with (a) the transconductance parameter and (b) the current gain parameter

Small Signal Hybrid-π Equivalent Circuit for PNP BJT

$$V_o = (g_m V_\pi)(r_o \| R_C)$$

$$V_\pi = -\frac{V_s r_\pi}{R_B + r_\pi}$$

$$A_v = \frac{V_o}{V_s} = \frac{-g_m r_\pi}{R_B + r_\pi}(r_o \| R_C) = \frac{-\beta}{R_B + r_\pi}(r_o \| R_C)$$

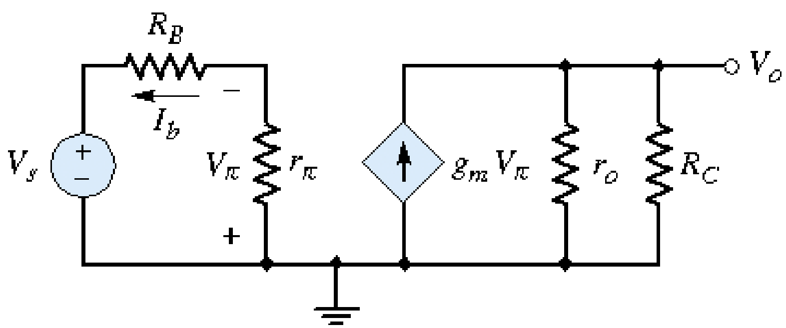


Figure 4.16 The small-signal equivalent circuit of the common-emitter circuit with a pnp transistor

EXAMPLE 6.3

Objective: Analyze a pnp amplifier circuit.

Consider the circuit shown in Figure 6.18. Assume transistor param $\beta = 80$, $V_{EB}(\text{on}) = 0.7$ V, and $V_A = \infty$.

Solution (DC Analysis): A dc KVL equation around the E–B loop yields

$$V^+ = V_{EB}(\text{on}) + I_{BQ}R_B + V_{BB}$$

or

$$5 = 0.7 + I_{BQ}(50) + 3.65$$

which yields

$$I_{BQ} = 13\ \mu\text{A}$$

Then

$$I_{CQ} = 1.04\ \text{mA} \qquad I_{EQ} = 1.05\ \text{mA}$$

A dc KVL equation around the E–C loop yields

$$V^+ = V_{ECQ} + I_{CQ}R_C$$

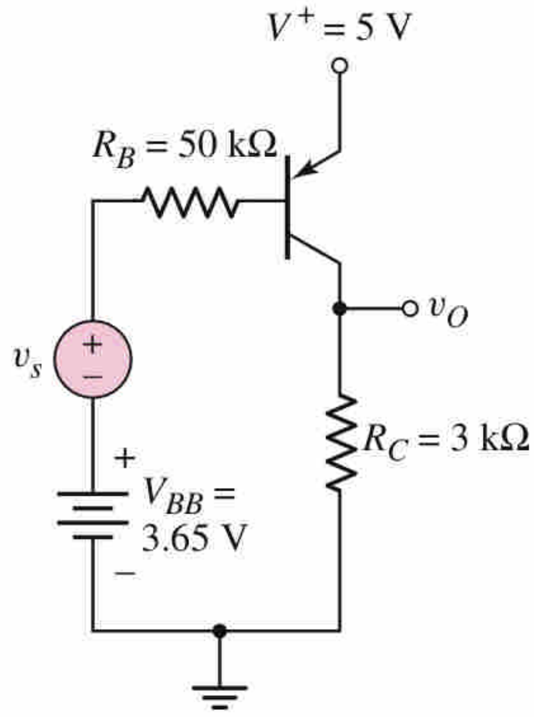
or

$$5 = V_{ECQ} + (1.04)(3)$$

We find

$$V_{ECQ} = 1.88\ \text{V}$$

The transistor is therefore biased in the forward-active mode.



Solution (AC Analysis): The small-signal hybrid-π parameters are found to

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.04}{0.026} = 40\,\text{mA/V}$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(80)(0.026)}{1.04} = 2\,\text{k}\Omega$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{\infty}{1.04} = \infty$$

The small-signal equivalent circuit is the same as shown in Figure 6.17. With r the small-signal output voltage is

$$V_o = (g_m V_\pi) R_C$$

and we have

$$V_\pi = -\left(\frac{r_\pi}{r_\pi + R_B}\right) \cdot V_s$$

Noting that $\beta = g_m r_\pi$, we find the small-signal voltage gain to be

$$A_v = \frac{V_o}{V_s} = \frac{-\beta R_C}{r_\pi + R_B} = \frac{-(80)(3)}{2 + 50}$$

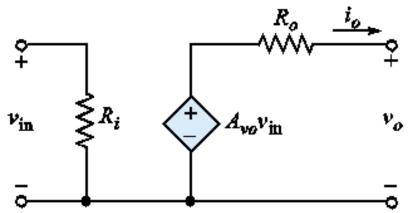
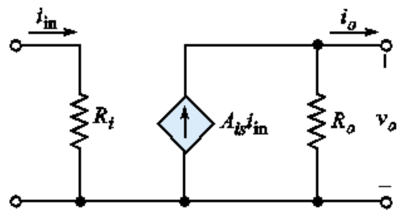
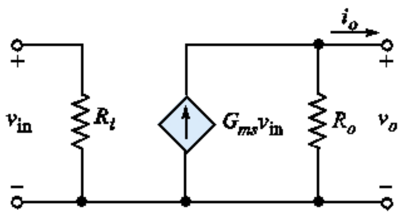
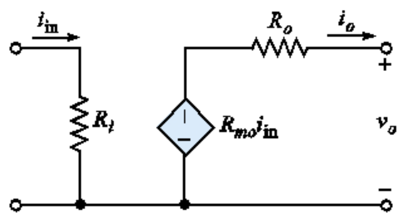
or

$$A_v = -4.62$$

Comment: We again note the $-180°$ phase shift between the output and input signals. We may also note that the base resistance R_B in the denominator substantially reduces the magnitude of the small-signal voltage gain. We can also note that placing the pnp transistor in this configuration allows us to use positive power supplies.

Two Port Network Model

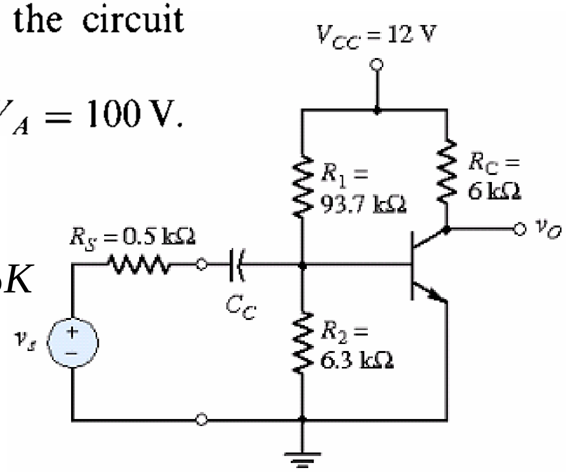
Table 4.3 Four equivalent two-port networks

Type	Equivalent circuit	Gain property
Voltage amplifier		Output voltage proportional to input voltage
Current amplifier		Output current proportional to input current
Transconductance amplifier		Output current proportional to input voltage
Transresistance amplifier		Output voltage proportional to input current

Common-Emitter Amplifier

Example 4.4 **Objective:** Determine the small-signal voltage gain of the circuit shown in Figure 4.25.

Assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$.



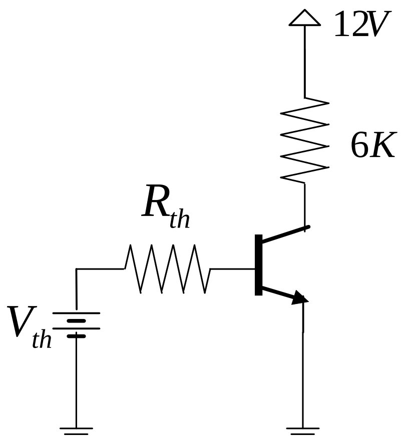
A. DC analysis

$$V_{th} = \frac{6.3}{93.7+6.3} \times 12 = 0.756V$$

$$R_{th} = 93.7K // 6.3K = 5.9K$$

$$I_B = \frac{0.756-0.7}{5.9K} = 9.5\mu A$$

$$I_C = 100 I_B = 0.95mA$$



B. AC analysis

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = 100 \times \frac{0.026}{0.95} \times 10^3 = 2.736K$$

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{0.95} \times 10^3 = 105K$$

$$i_b = \frac{v_\pi}{r_\pi} = \frac{1}{r_\pi} \times \frac{6.3//93.7//r_\pi}{6.3//93.7//r_\pi + 0.5} v_s = 0.288 v_s$$

$$v_o = -\beta\, i_b \times (r_o // R_C) = -100 \times 0.288 v_s \times 5.67 = -163.23 v_s$$

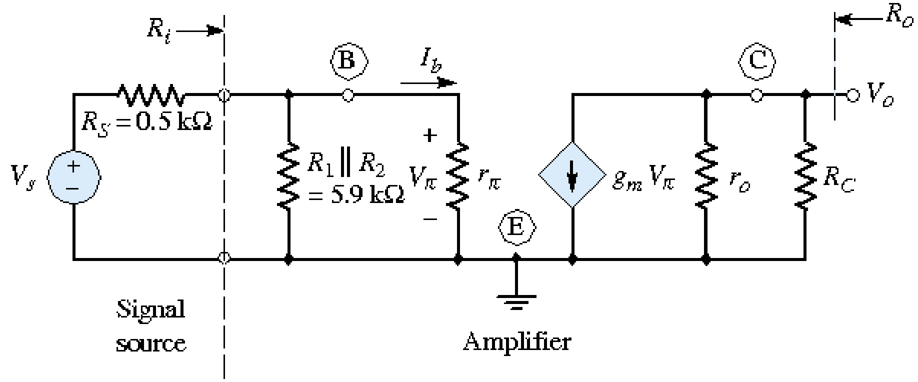


Figure 4.26 The small-signal equivalent circuit, assuming the coupling capacitor is a short circuit

Common Emitter amplifier

Discussion: The two-port equivalent circuit along with the input signal source for the common-emitter amplifier analyzed in this example is shown in Figure 4.27. We can determine the effect of the source resistance R_S in conjunction with the amplifier input resistance R_i. Using a voltage-divider equation, we find the input voltage to the amplifier is

$$V_{\text{in}} = \left(\frac{R_i}{R_i + R_S}\right) V_s = \left(\frac{1.87}{1.87 + 0.5}\right) V_s = 0.789 V_s$$

Because the input resistance to the amplifier is not very much greater than the signal source resistance, the actual input voltage to the amplifier is reduced to approximately 80 percent of the signal voltage. This is called a **loading effect**. The voltage V_{in} is a function of the amplifier connected to the source. In other amplifier designs, we will try to minimize the loading effect, or make $R_i \gg R_S$, which means that $V_{\text{in}} \cong V_s$.

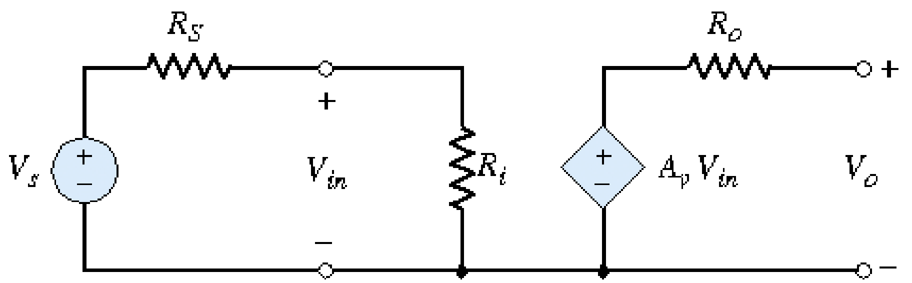
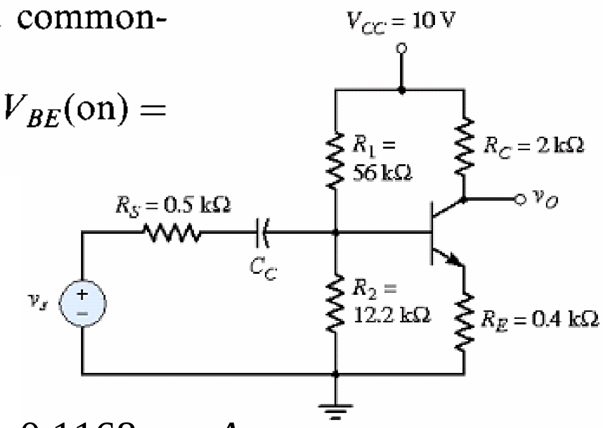


Figure 4.27 Two-port equivalent circuit for the amplifier in Example 4.4

Common-Emitter Circuit with Emitter Resistor

Example 4.5 **Objective:** Determine the small-signal voltage gain of a common-emitter circuit with an emitter resistor.

For the circuit in Figure 4.28, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$.



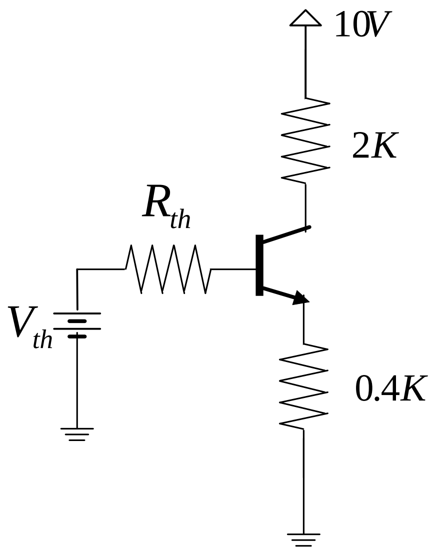
A. DC analysis

$$V_{th} = \frac{12.2}{56+12.2} \times 10 = 1.79V$$

$$R_{th} = 56K // 12.2K = 10K$$

$$I_B = \frac{1.79-0.7}{10+(1+100)\times 0.4} = 0.0216mA$$

$$I_C = 100 I_B = 2.16mA$$



B. AC analysis

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = 100 \times \frac{0.026}{2.16} = 1.2K$$

$$i_s = \frac{v_s}{10//(r_\pi + (1+\beta)\times 0.4) + 0.5} = 0.1168 v_s, mA$$

$$i_b = \frac{10}{10+(r_\pi + (1+\beta)\times 0.4)} \times i_s = 0.1938 i_s, mA$$

$$v_o = -\beta\, i_b \times R_C = -100 \times 0.1938 \times 0.1168 v_s \times 2 = -4.527 v_s$$

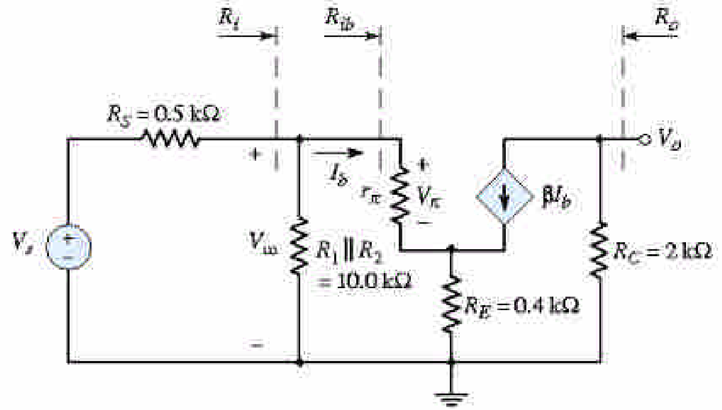


Figure 4.29 The small-signal equivalent circuit with an emitter resistor

Amplification Stability

The input resistance to the amplifier is now

$$R_i = R_1 \| R_2 \| R_{ib} \tag{4.48}$$

We can again relate V_{in} to V_s through a voltage-divider equation as

$$V_{in} = \left(\frac{R_i}{R_i + R_S}\right) \cdot V_s \tag{4.49}$$

Combining Equations (4.45), (4.47), and (4.49), we find the small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = \frac{-(\beta I_b)R_C}{V_s} = -\beta R_C\left(\frac{V_{in}}{R_{ib}}\right) \cdot \left(\frac{1}{V_s}\right) \tag{4.50(a)}$$

or

$$A_v = \frac{-\beta R_C}{r_\pi + (1+\beta)R_E}\left(\frac{R_i}{R_i + R_S}\right) \tag{4.50(b)}$$

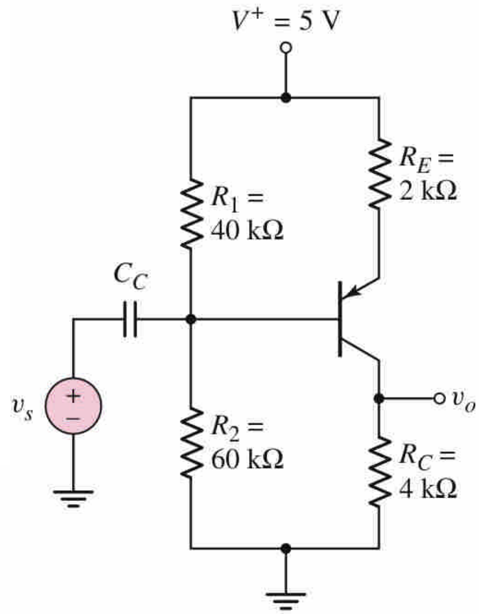
From this equation, we see that if $R_i \gg R_S$ and if $(1+\beta)R_E \gg r_\pi$, then the small-signal voltage gain is approximately

$$A_v \cong \frac{-\beta R_C}{(1+\beta)R_E} \cong \frac{-R_C}{R_E} \quad \text{..... independent of } \beta \tag{4.51}$$

EXAMPLE 6.7

Objective: Analyze a pnp transistor circuit.

Consider the circuit shown in Figure 6.34(a). Determine the quiescent p meter values and then the small-signal voltage gain. The transistor parameters $V_{EB}(\text{on}) = 0.7$ V, $\beta = 80$, and $V_A = \infty$.



Solution (dc Analysis): The dc equivalent circuit with the Thevenin equivalent c cuit of the base biasing is shown in Figure 6.34(b). We find

$$R_{TH} = R_1 \| R_2 = 40 \| 60 = 24\,\text{k}\Omega$$

and

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) \cdot V^+ = \left(\frac{60}{60 + 40}\right)(5) = 3\text{ V}$$

Writing a KVL equation around the E–B loop, assuming the transistor is biased in forward-active mode, we find

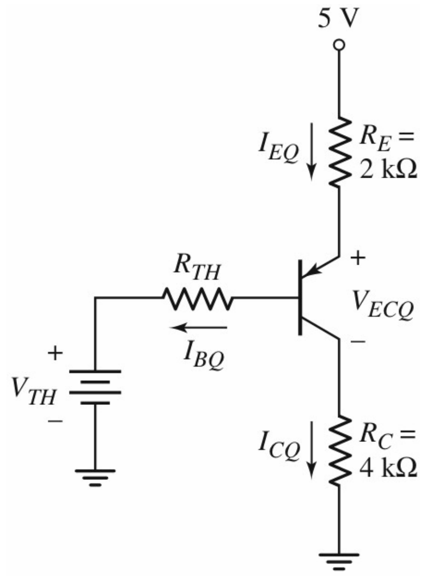
$$V^+ = (1 + \beta) I_{BQ} R_E + V_{EB}(\text{on}) + I_{BQ} R_{TH} + V_{TH}$$

Solving for the base current, we obtain

$$I_{BQ} = \frac{V^+ - V_{EB}(\text{on}) - V_{TH}}{R_{TH} + (1 + \beta) R_E} = \frac{5 - 0.7 - 3}{24 + (81)(2)}$$

or

$$I_{BQ} = 0.00699\,\text{mA}$$



Then

$$I_{CQ} = \beta I_{BQ} = 0.559 \text{ mA}$$

and

$$I_{EQ} = (1+\beta)I_{BQ} = 0.566 \text{ mA}$$

The quiescent emitter-collector voltage is

$$V_{ECQ} = V^+ - I_{EQ}R_E - I_{CQ}R_C = 5 - (0.566)(2) - (0.559)(4)$$

or

$$V_{ECQ} = 1.63 \text{ V}$$

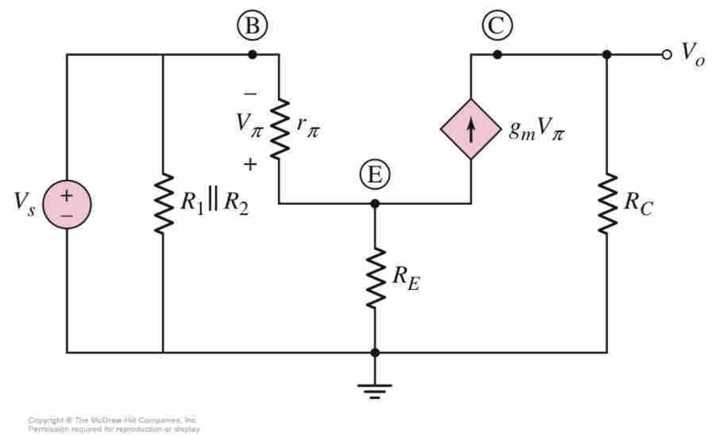
Solution (ac analysis): The small-signal hybrid-π parameters are as follows:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(80)(0.026)}{0.559} = 3.72 \text{ k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.559}{0.026} = 21.5 \text{ mA/V}$$

and

$$r_o = \frac{V_A}{I_Q} = \infty$$



The small-signal equivalent circuit is shown in Figure 6.35. As noted before, we start with the three terminals of the transistor, sketch the hybrid-π equivalent circuit between these three terminals, and then put in the other circuit elements around the transistor.

The output voltage is

$$V_o = g_m V_\pi R_C$$

Writing a KVL equation from the input around the B–E loop, we find

$$V_s = -V_\pi - \left(\frac{V_\pi}{r_\pi} + g_m V_\pi\right) R_E$$

The term in the parenthesis is the total current through the R_E resistor. Solvingf and recalling that $g_m r_\pi = \beta$, we obtain

$$V_\pi = \frac{-V_s}{1 + \left(\frac{1+\beta}{r_\pi}\right) R_E}$$

Substituting into the expression for the output voltage, we find the small-signal age gain as

$$A_v = \frac{V_o}{V_s} = \frac{-\beta R_C}{r_\pi + (1+\beta) R_E}$$

Then

$$A_v = \frac{-(80)(4)}{3.72 + (81)(2)} = -1.93$$

The negative sign indicates that the output voltage is 180 degrees out of phase respect to the input voltage. This same result was found in common-emitter ci using npn transistors.

Using the approximation given by Equation (6.59), we have

$$A_v \cong -\frac{R_C}{R_E} = -\frac{4}{2} = -2$$

This approximation is very close to the actual value of gain calculated.

Common Emitter Circuit with Emitter Bypass Capacitor

- We can use an emitter bypass capacitor to effectively short out a portion or all of the emitter resistance to enhance the small-signal voltage gain.

Design Example 4.6 **Objective:** An amplifier with the configuration in Figure 4.32 is to be designed such that a 12 mV sinusoidal signal from a microphone is amplified to a 0.4 V sinusoidal output signal. Standard resistor values are to be used in the final design.

Initial Design Approach: The magnitude of the voltage gain of the amplifier needs to be

$$|A_v| = \frac{0.4\,\text{V}}{12\,\text{mV}} = 33.3$$

From Equation (4.51), the approximate voltage gain of the amplifier is

$$|A_v| \cong \frac{R_C}{R_{E1}}$$

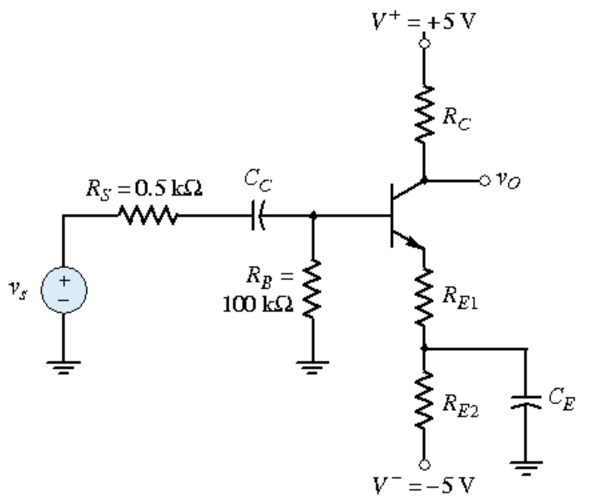


Figure 4.32 A bipolar circuit with an emitter resistor and an emitter bypass capacitor

Noting from the last example that this value of gain produces an optimistically high value, we can set $R_C/R_{E1} = 40$ or $R_C = 40R_{E1}$.

The dc base-emitter loop equation is

$$5 = I_B R_B + V_{BE}(\text{on}) + I_E(R_{E1} + R_{E2})$$

Assuming $\beta = 100$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$, we can design the circuit to produce a quiescent emitter current of, for example, 0.20 mA. We then have

$$5 = \frac{(0.20)}{(101)}(100) + 0.70 + (0.20)(R_{E1} + R_{E2})$$

which yields

$$R_{E1} + R_{E2} = 20.5\,\text{k}\Omega$$

Assuming $I_E \cong I_C$ and designing the circuit such that $V_{CEQ} = 4\,\text{V}$, the collector–emitter loop equation produces

$$5 + 5 = I_C R_C + V_{CEQ} + I_E(R_{E1} + R_{E2}) = (0.2)R_C + 4 + (0.2)(20.5)$$

or

$$R_C = 9.5\,\text{k}\Omega$$

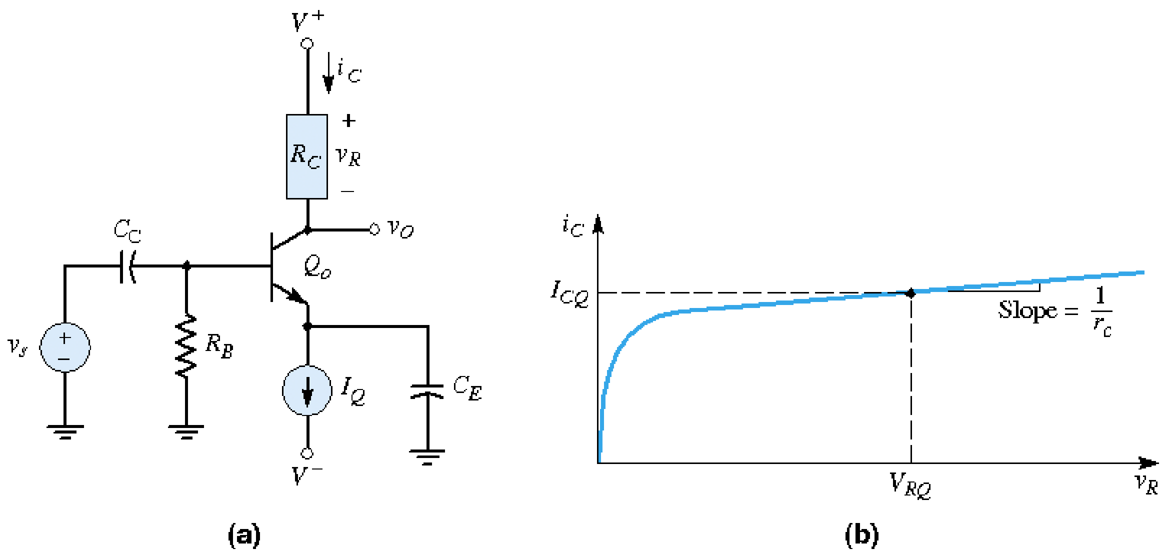
Then

$$R_{E1} = \frac{R_C}{40} = \frac{9.5}{40} = 0.238\,\text{k}\Omega$$

and $R_{E2} = 20.3\,\text{k}\Omega$.

From Appendix D, we can pick standard resistor values of $R_{E1} = 240\,\Omega$, $R_{E2} = 20\,\text{k}\Omega$, and $R_C = 10\,\text{k}\Omega$.

Common-Emitter Circuit with Current Source



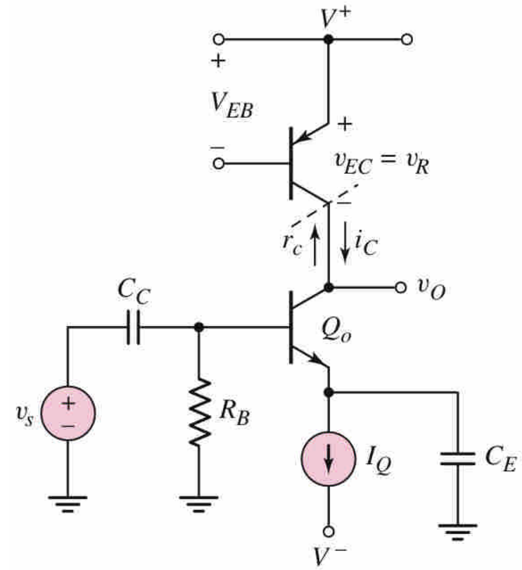


Figure 4.37 (a) A common-emitter circuit with current source biasing and a nonlinear load resistor and (b) current–voltage characteristics of the nonlinear load resistor

$$A_v = \frac{V_o}{V_s} = -g_m(r_o \| r_c) \qquad (4.52)$$

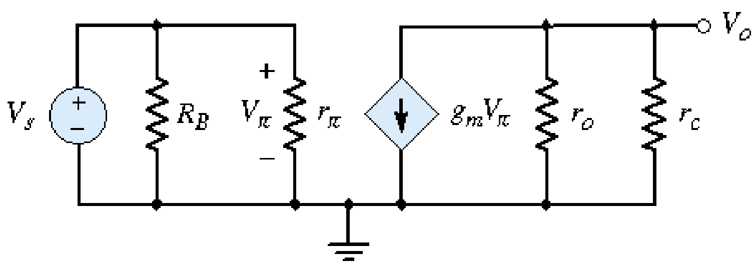


Figure 4.38 Small-signal equivalent circuit of the circuit in Figure 4.37(a)

Example 4.7 **Objective:** Determine the small-signal voltage gain of a common-emitter circuit with a nonlinear load resistance.

Assume the circuit shown in Figure 4.37(a) is biased at $I_Q = 0.5\,\text{mA}$, and the transistor parameters are $\beta = 120$ and $V_A = 80\,\text{V}$. Also assume that nonlinear small-signal collector resistance is $r_c = 120\,\text{k}\Omega$.

Solution: For a transistor current gain of $\beta = 120$, $I_{CQ} \cong I_{EQ} = I_Q$, and the small-signal hybrid-π parameters are

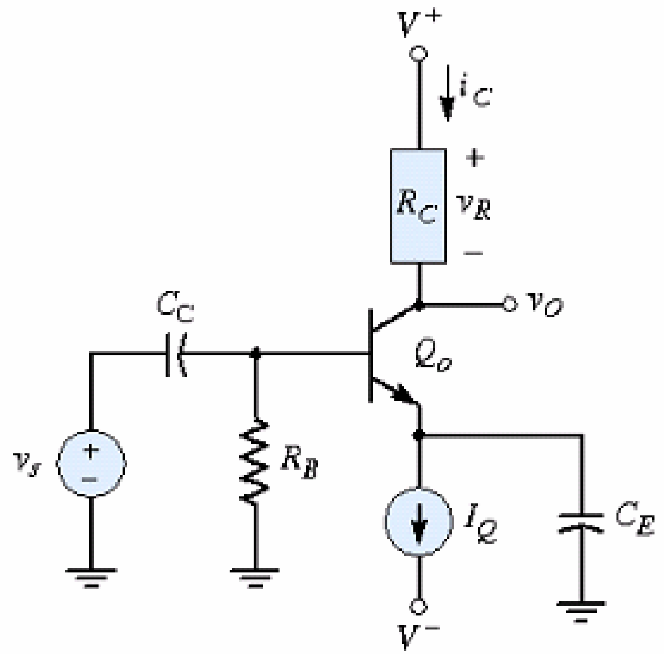
$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.5}{0.026} = 19.2\,\text{mA/V}$$

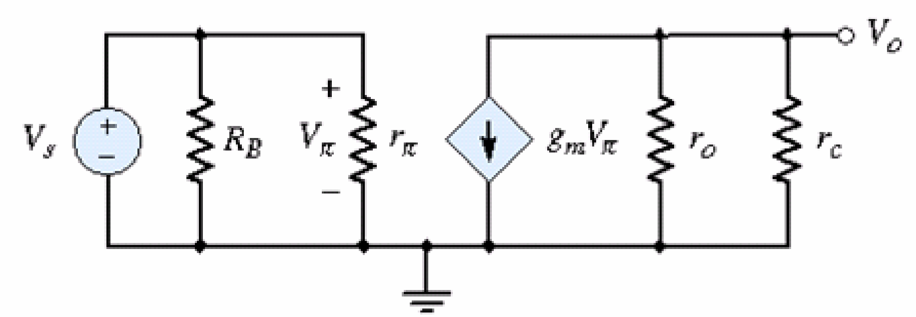
and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{80}{0.5} = 160\,\text{k}\Omega$$

The small-signal voltage gain is therefore

$$A_v = -g_m(r_o \| r_c) = -(19.2)(160\|120) = -1317$$





AC Load Line

DC Load Line:

$$V^+ = I_C R_C + V_{CE} + I_E(R_{E1} + R_{E2}) + V^-$$

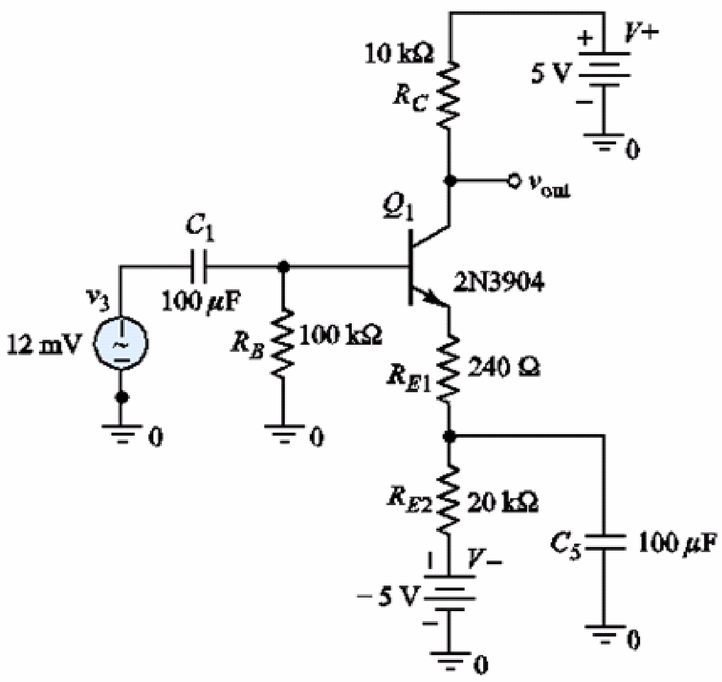
$$I_E = [(1+\beta)/\beta] I_C$$

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)(R_{E1} + R_{E2})\right]$$

AC Load Line:

$$i_c R_C + v_{ce} + i_e R_{E1} = 0$$

$$\text{assuming } i_c \cong i_e,\ v_{ce} = -i_c(R_C + R_{E1})$$



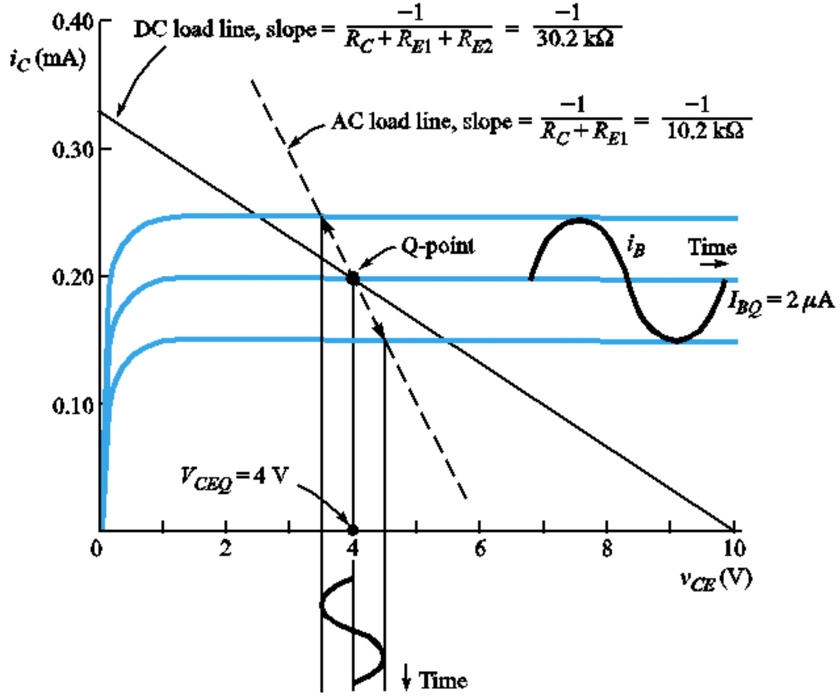


Figure 4.39 The dc and ac load lines for the circuit in Figure 4.33, and the signal responses to input signal

Example 4.8 **Objective:** Determine the dc and ac load lines for the circuit shown in Figure 4.40.

Assume the transistor parameters are: $V_{EB}(\text{on}) = 0.7\,\text{V}$, $\beta = 150$, and $V_A = \infty$.

DC Solution: The dc load line is found by writing a KVL equation around the C–E loop, as follows:

$$V^+ = I_E R_E + V_{EC} + I_C R_C + V^-$$

The dc load line equation is then

$$V_{EC} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right]$$

Assuming that $(1+\beta)/\beta \cong 1$, the dc load line is plotted in Figure 4.41.

To determine the Q-point parameters, write a KVL equation around the B–E loop, as follows:

$$V^- = (1+\beta)I_{BQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_B$$

or

$$I_{BQ} = \frac{V^+ - V_{EB}(\text{on})}{R_B + (1+\beta)R_E} = \frac{10 - 0.7}{50 + (151)(10)} \Rightarrow 5.96\,\mu\text{A}$$

Then,

$$I_{CQ} = \beta I_{BQ} = (150)(5.96\,\mu\text{A}) \Rightarrow 0.894\,\text{mA}$$
$$I_{EQ} = (1+\beta)I_{BQ} = (151)(5.96\,\mu\text{A}) \Rightarrow 0.90\,\text{mA}$$

and

$$V_{ECQ} = (V^+ - V^-) - I_{CQ}R_C - I_{EQ}R_E$$
$$= [10 - (-10)] - (0.894)(5) - (0.90)(10) = 6.53\,\text{V}$$

The Q-point is also plotted in Figure 4.41.

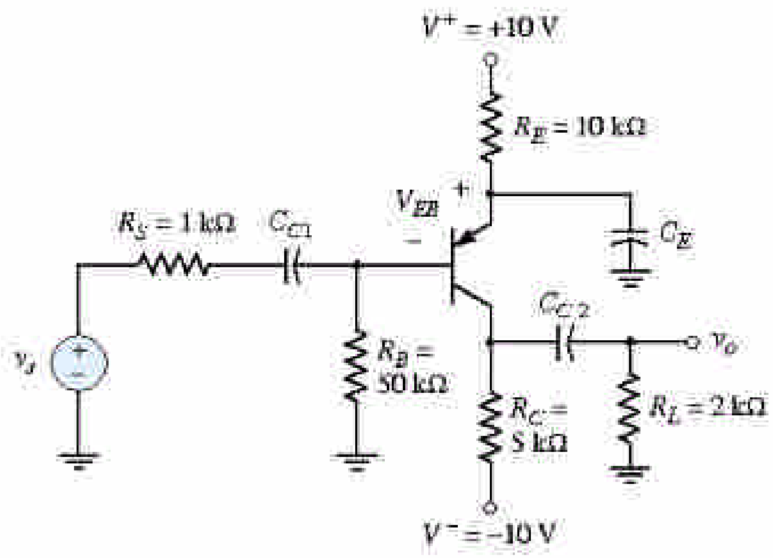


Figure 4.40 Circuit for Example 4.8

AC Solution: Assuming that all capacitors act as short circuits, the small-signal equivalent circuit is shown in Figure 4.42. Note that the current directions and voltage polarities in the hybrid-π equivalent circuit of the pnp transistor are reversed compared to those of the npn device. The small-signal hybrid-π parameters are

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(150)}{0.894} = 4.36\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.894}{0.026} = 34.4\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{\infty}{I_{CQ}} = \infty$$

The small-signal output voltage, or C–E voltage, is

$$v_o = v_{ce} = +(g_m v_\pi)(R_C \| R_L)$$

where

$$g_m v_\pi = i_c$$

The ac load line, written in terms of the E–C voltage, is defined by

$$v_{ec} = -i_c(R_C \| R_L)$$

The ac load line is also plotted in Figure 4.41.

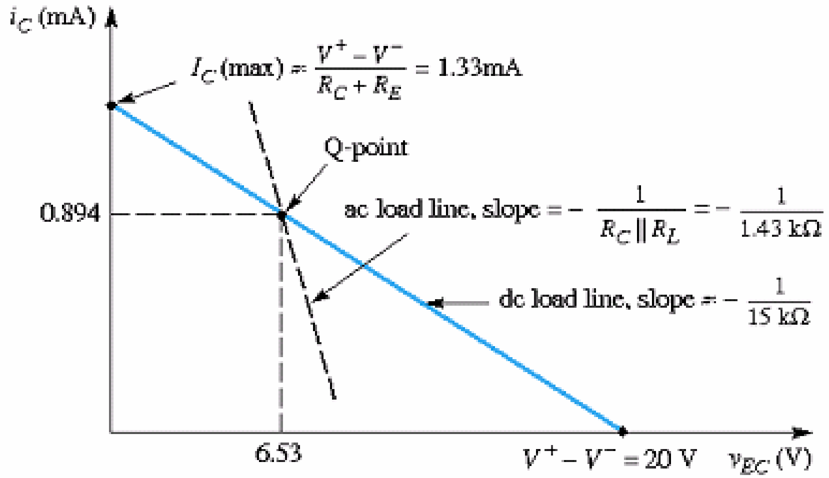


Figure 4.41 Plots of dc and ac load lines for Example 4.8

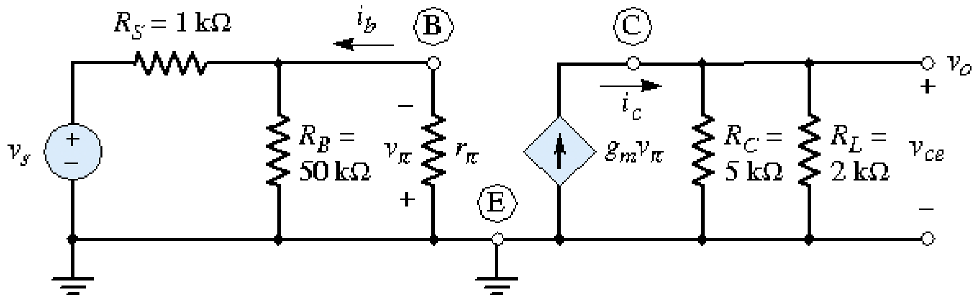


Figure 4.42 The small-signal equivalent circuit for Example 4.8

Maximum Symmetrical Swing

- When symmetrical sinusoidal signals are applied to the input of an amplifier, symmetrical sinusoidal signals are generated at the output.
- AC load can be used to determine the maximum output symmetrical swing.
- If the output exceeds the limit, a portion of the output signal will be clipped and signal distortion will occurs.

Example 4.9 **Objective:** Determine the maximum symmetrical swing in the output voltage of the circuit given in Figure 4.40.

Solution: The ac load line is given in Figure 4.41. The maximum negative swing in the collector current is from 0.894 mA to zero; therefore, the maximum possible symmetrical peak-to-peak ac collector current is

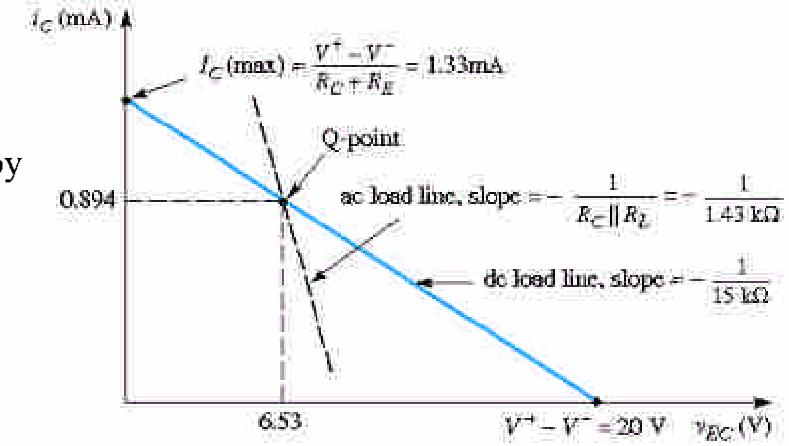
$$\Delta i_c = 2(0.894) = 1.79\,\text{mA}$$

The maximum symmetrical peak-to-peak output voltage is given by

$$|\Delta v_{ec}| = |\Delta i_c|(R_C \| R_L) = (1.79)(5\|2) = 2.56\,\text{V}$$

Therefore, the maximum instantaneous collector current is

$$i_C = I_{CQ} + \tfrac{1}{2}|\Delta i_c| = 0.894 + 0.894 = 1.79\,\text{mA}$$



Comment: Considering the Q-point and the maximum swing in the C–E voltage, the transistor remains biased in the forward-active region. Note that the maximum instantaneous collector current, 1.79 mA, is larger than the maximum dc collector current, 1.33 mA, as determined from the dc load line. This apparent anomaly is due to the different resistance in the C–E circuit for the ac signal and the dc signal.

DESIGN EXAMPLE 6.12

Objective: Design a circuit to achieve a maximum symmetrical swing in the output voltage.

Specifications: The circuit configuration to be designed is shown in Figure 6.48a. The circuit is to be designed to be bias stable. The minimum collector current is to be $I_C(\text{min}) = 0.1$ mA and the minimum collector-emitter voltage is to be $V_{CE}(\text{min}) = 1$ V.

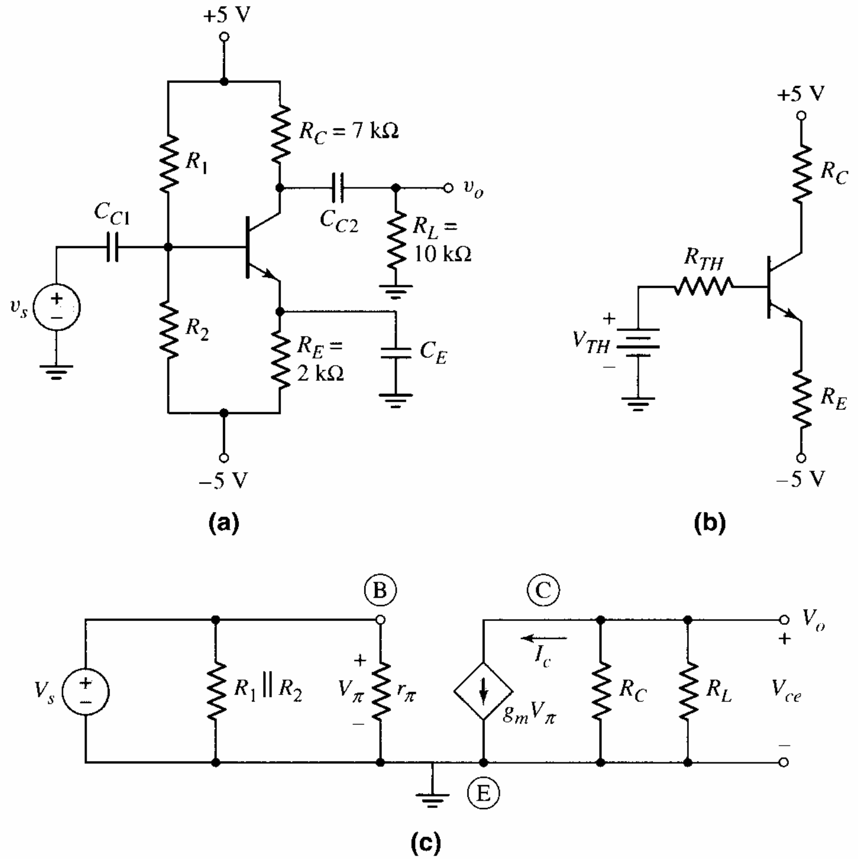


Figure 6.48 (a) Circuit for Example 6.12, (b) Thevenin equivalent circuit, and (c) small-signal equivalent circuit

Choices: Assume nominal resistance values of $R_E = 2\,\text{k}\Omega$ and $R_C = 7\,\text{k}\Omega$. Let $R_{TH} = R_1 \| R_2 = (0.1)(1+\beta)R_E = 24.2\,\text{k}\Omega$. Assume transistor parameters of $\beta = 120$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$.

Solution (Q-Point): The dc equivalent circuit is shown in Figure 6.48(b) and the midband small-signal equivalent circuit is shown in Figure 6.48(c).

The dc load line, from Figure 6.48(b), is (assuming $I_C \cong I_E$)

$$V_{CE} = 10 - I_C(R_C + R_E) = 10 - I_C(9)$$

The ac load line, from Figure 6.48(c), is

$$V_{ce} = -I_c(R_C \| R_L) = -I_c(4.12)$$

These two load lines are plotted in Figure 6.49. At this point, the Q-point is unknown. Also shown in the figure are the $I_C(\text{min})$ and $V_{CE}(\text{min})$ values. The peak value of the ac collector current is ΔI_C and the peak value of the ac collector–emitter voltage is ΔV_{CE}.

We can write

$$\Delta I_C = I_{CQ} - I_C(\text{min}) = I_{CQ} - 0.1$$

and

$$\Delta V_{CE} = V_{CEQ} - V_{CE}(\text{min}) = V_{CEQ} - 1$$

where $I_C(\text{min})$ and $V_{CE}(\text{min})$ were given in the specifications.

Now

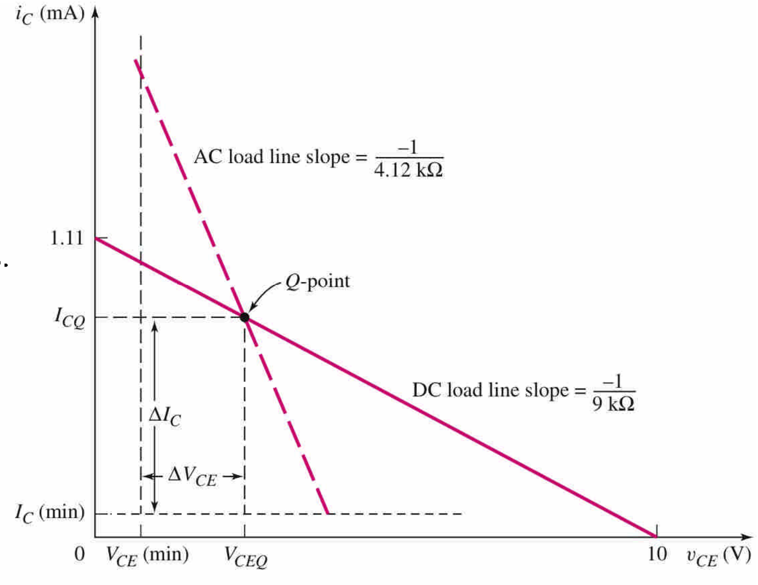
$$\Delta V_{CE} = \Delta I_C(R_C \| R_L)$$

or

$$V_{CEQ} - 1 = (I_{CQ} - 0.1)(4.12)$$

Substituting the expression for the dc load line, we obtain

$$10 - I_{CQ}(9) - 1 = (I_{CQ} - 0.1)(4.12)$$



which yields

$$I_{CQ} = 0.717\,\text{mA}$$

and then

$$V_{CEQ} = 3.54\,\text{V}$$

Solution (Bias Resistors): We can now determine R_1 and R_2 to produce the desired Q-point.

From the dc equivalent circuit, we have

$$\begin{aligned} V_{TH} &= \left(\frac{R_2}{R_1 + R_2}\right)[5 - (-5)] - 5 \\ &= \frac{1}{R_1}(R_{TH})(10) - 5 = \frac{1}{R_1}(24.2)(10) - 5 \end{aligned}$$

Then, from a KVL equation around the B–E loop, we obtain

$$V_{TH} = \left(\frac{I_{CQ}}{\beta}\right) R_{TH} + V_{BE}(\text{on}) + \left(\frac{1+\beta}{\beta}\right) I_{CQ} R_E - 5$$

or

$$\frac{1}{R_1}(24.2)(10) - 5 = \left(\frac{0.717}{120}\right)(24.2) + 0.7 + \left(\frac{121}{120}\right)(0.717)(2) - 5$$

which yields

$$R_1 = 106\,\text{k}\Omega$$

We then find

$$R_2 = 31.4\,\text{k}\Omega$$

Symmetrical Swing Results: We then find that the peak ac collector current is $\Delta I_C = 0.617$ mA, or the peak-to-peak ac collector current is 1.234 mA. The peak ac collect-emitter voltage is 2.54 V, or the peak-to-peak ac collector-emitter voltage is 5.08 V.

Common-Collector Amplifier (Emitter-Follower)

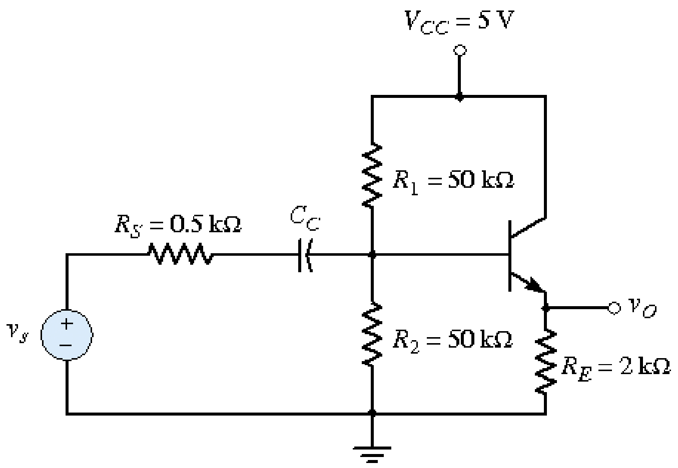


Figure 4.44 Emitter-follower circuit

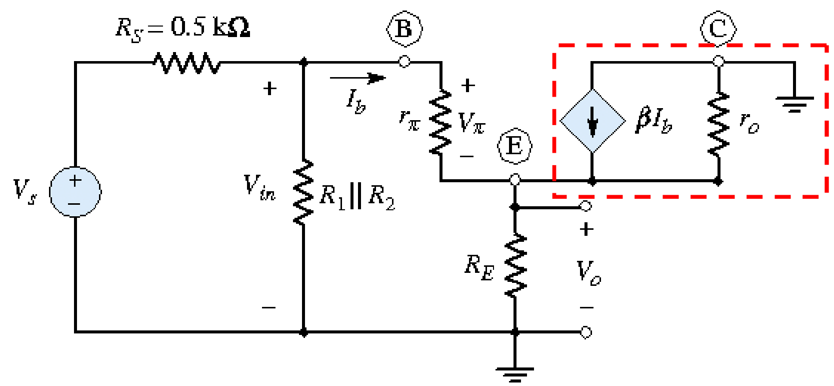


Figure 4.45 Small-signal equivalent circuit of the emitter-follower

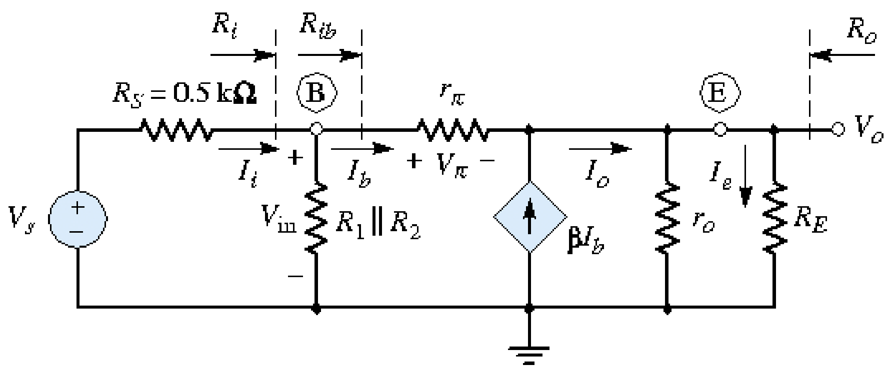


Figure 4.46 Another small-signal equivalent circuit for the emitter-follower

Common-Collector Amplifier (Emitter-Follower)

- Small-Signal Voltage Gain

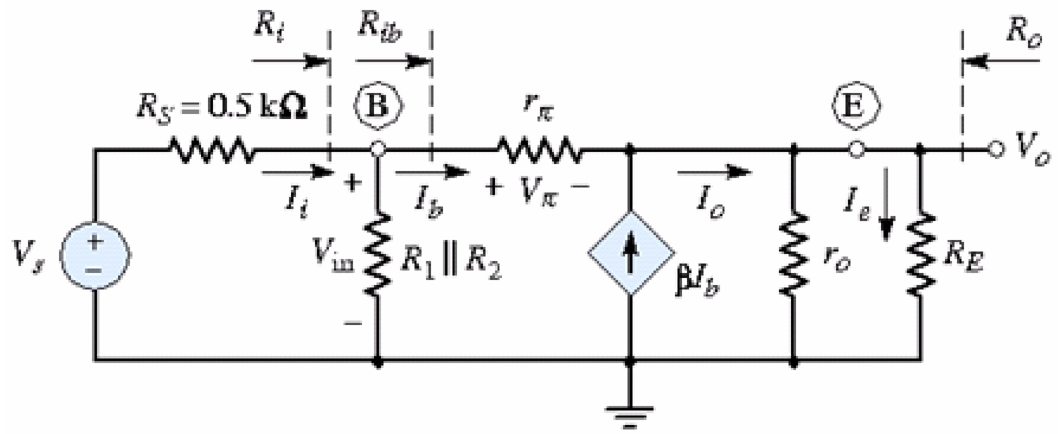
I_b :Base Input Current

$$V_o = I_b(1+\beta)(r_o // R_E)$$

$$R_{ib} = r_\pi + (1+\beta)(r_o // R_E)$$

$$I_b = V_b / R_{ib} \quad (V_b = V_{in})$$

$$V_o = \frac{(1+\beta)(r_o // R_E)}{r_\pi + (1+\beta)(r_o // R_E)} V_b$$



$$V_b = \frac{R_i}{R_s + R_i} V_s$$

$$R_i = R_1 // R_2 // R_{ib}$$

$$A_v = \frac{V_o}{V_s} = \frac{(1+\beta)(r_o // R_E)}{r_\pi + (1+\beta)(r_o // R_E)} \frac{R_1 // R_2 // R_{ib}}{R_s + R_1 // R_2 // R_{ib}}$$

Example 4.10 **Objective:** Calculate the small-signal voltage gain of an emitter-follower circuit.

For the circuit shown in Figure 4.44, assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 80\,\text{V}$.

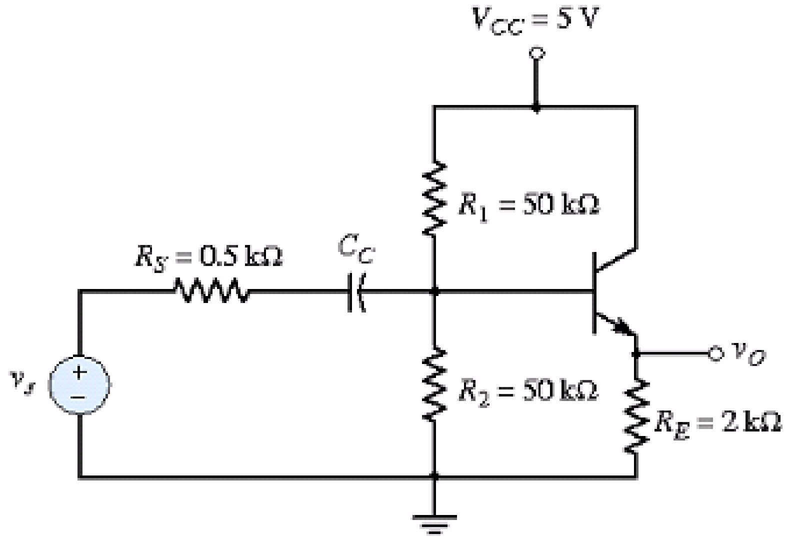
Solution: The dc analysis shows that $I_{CQ} = 0.793\,\text{mA}$ and $V_{CEQ} = 3.4\,\text{V}$. The small-signal hybrid-π parameters are determined to be

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(100)}{0.793} = 3.28\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.793}{0.026} = 30.5\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{80}{0.793} \cong 100\,\text{k}\Omega$$



We may note that

$$R_{ib} = 3.28 + (101)(100\|2) = 201\,\text{k}\Omega$$

and

$$R_i = 50\|50\|201 = 22.2\,\text{k}\Omega$$

The small-signal voltage gain is then

$$A_v = \frac{(101)(100\|2)}{3.28 + (101)(100\|2)} \cdot \left(\frac{22.2}{22.2 + 0.5}\right)$$

or

$$A_v = +0.962$$

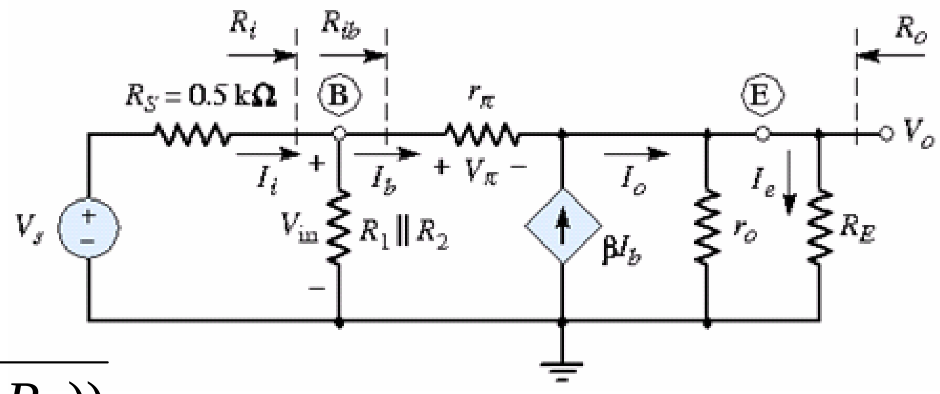
Common-Collector Amplifier (Emitter-Follower)

- Input Impedance

$$R_{ib} = r_\pi + (1+\beta)(r_o \,//\, R_E)$$

$$R_i = R_1 \,//\, R_2 \,//\, R_{ib}$$

$$I_i = \frac{V_s}{R_s + R_1 \,//\, R_2 \,//(r_\pi + (1+\beta)(r_o \,//\, R_E))}$$



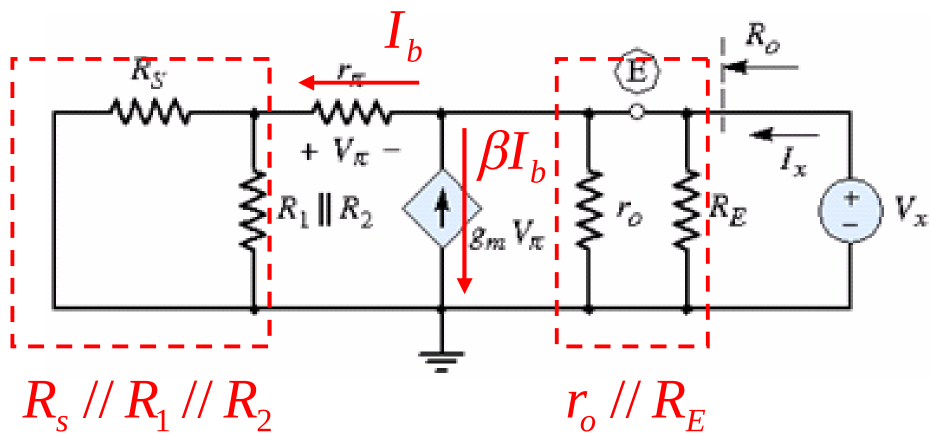
- Output Impedance

$$I_b = \frac{V_x}{r_\pi + R_s \,//\, R_1 \,//\, R_2}$$

$$I_x = \frac{V_x}{r_o \,//\, R_E} + (1+\beta)\frac{V_x}{r_\pi + R_s \,//\, R_1 \,//\, R_2}$$

$$\frac{1}{R_o} = \frac{I_x}{V_x}$$

$$R_o = \left(\frac{r_\pi + R_s \,//\, R_1 \,//\, R_2}{1+\beta}\right) // \, r_o \,//\, R_E$$



Example 4.11 **Objective:** Calculate the input and output resistance of the emitter-follower circuit shown in Figure 4.44.

The small-signal parameters, as determined in Example 4.10, are $r_\pi = 3.28\,\text{k}\Omega$, $\beta = 100$, and $r_o = 100\,\text{k}\Omega$.

Solution: **Input Resistance**. The input resistance looking into the base was determined in Example 4.10 as

$$R_{ib} = r_\pi + (1+\beta)(r_o \| R_E) = 3.28 + (101)(100\|2) = 201\,\text{k}\Omega$$

and the input resistance seen by the signal source R_i is

$$R_i = R_1 \| R_2 \| R_{ib} = 50\|50\|201 = 22.2\,\text{k}\Omega$$

Solution: **Output Resistance**. The output resistance is found from Equation (4.66) as

$$R_o = \left(\frac{r_\pi + R_1\|R_2\|R_S}{1+\beta}\right)\|R_E\|r_o = \left(\frac{3.28 + 50\|50\|0.5}{101}\right)\|2\|100$$

or

$$R_o = 0.0373\|2\|100 = 0.0366\,\text{k}\Omega \Rightarrow 36.6\,\Omega$$

The output resistance is dominated by the first term that has $(1+\beta)$ in the denominator.

Comment: The emitter-follower circuit is sometimes referred to as an **impedance transformer**, since the input impedance is large and the output impedance is small. The very low output resistance makes the *emitter-follower act almost like an ideal voltage source,* so the output is not loaded down when used to drive another load. Because of this, the emitter-follower is often used as the output stage of a multistage amplifier.

Common-Collector Amplifier (Emitter-Follower)

- Small-Signal Current Gain

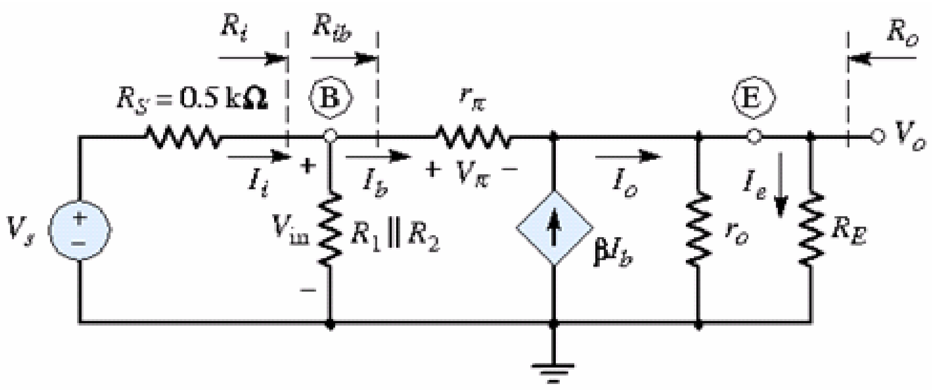
$$A_i = \frac{I_e}{I_i}$$

$$I_b = \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right) I_i$$

$$I_o = (1+\beta) I_b = (1+\beta)\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right) I_i$$

$$I_e = \left(\frac{r_o}{r_o + R_E}\right) I_o$$

$$A_i = \frac{I_e}{I_i} = (1+\beta)\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right)\left(\frac{r_o}{r_o + R_E}\right)$$



If we assume that $R_1 \| R_2 \gg R_{ib}$ and $r_o \gg R_E$, then

$$A_i \cong (1+\beta)$$

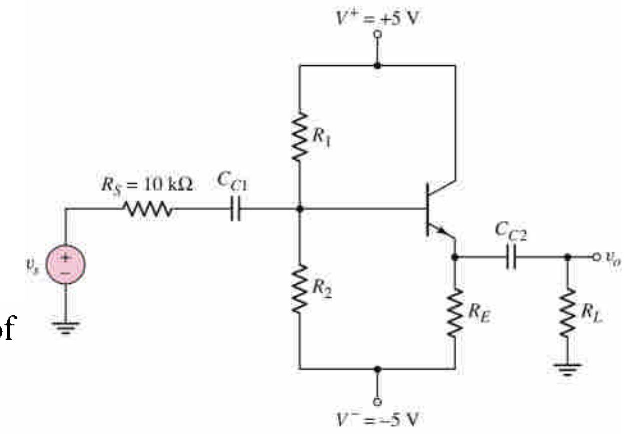
which is the current gain of the transistor.

Although the small-signal voltage gain of the emitter follower is slightly less than 1, the small-signal current is normally greater than 1. Therefore, the emitter-follower circuit produces a small-signal power gain.

DESIGN EXAMPLE 6.15

Objective: To design an emitter-follower amplifier to meet an output resis specification.

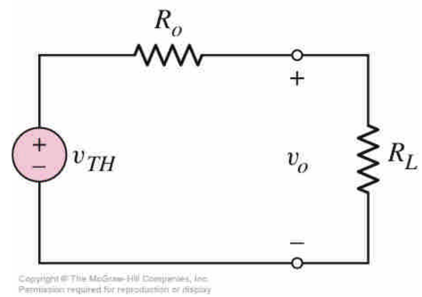
Specifications: Consider the output signal of the amplifier designed in Example 6.8. We now want to design an emitter-follower circuit with the configuration shown in Figure 6.57 such that the output signal from this circuit does not vary by more than 5 percent when a load in the range $R_L = 4\,\text{k}\Omega$ to $R_L = 20\,\text{k}\Omega$ is connected to the output.



Choices: We will assume that a transistor with nominal parameter values of $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 80$ V is available.

Discussion: The output resistance of the common-emitter circuit designed in Example 6.8 is $R_o = R_C = 10\,\text{k}\Omega$. Connecting a load resistance between $4\,\text{k}\Omega$ and $20\,\text{k}\Omega$ will load down this circuit, so that the output voltage will change substantially. For this reason, an emitter-follower circuit with a low output resistance must be designed to minimize the loading effect. The Thevenin equivalent circuit is shown in Figure 6.58. The output voltage can be written as

$$v_o = \left(\frac{R_L}{R_L + R_o}\right) \cdot v_{TH}$$



where v_{TH} is the ideal voltage generated by the amplifier. In order to have v_o change by less than 5 percent as a load resistance R_L is added, we must have R_o less than or equal to approximately 5 percent of the minimum value of R_L. In this case, then, we need R_o to be approximately 200 Ω.

Initial Design Approach: Consider the emitter-follower circuit shown in Figure 6.57. Note that the source resistance is $R_S = 10\,\text{k}\Omega$, corresponding to the output resistance of the circuit designed in Example 6.8. Assume that $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 80$ V.

The output resistance, given by Equation (6.79), is

$$R_o = \left(\frac{r_\pi + R_1 \| R_2 \| R_S}{1 + \beta}\right) \| R_E \| r_o$$

The first term, with $(1 + \beta)$ in the denominator, dominates, and if $R_1 \| R_2 \| R_S \cong R_S$, then we have

$$R_o \cong \frac{r_\pi + R_S}{1 + \beta}$$

For $R_o = 200\ \Omega$, we find

$$0.2 = \frac{r_\pi + 10}{101}$$

or $r_\pi = 10.2\ \text{k}\Omega$. Since $r_\pi = (\beta V_T)/I_{CQ}$, the quiescent collector current must be

$$I_{CQ} = \frac{\beta V_T}{r_\pi} = \frac{(100)(0.026)}{10.2} = 0.255\ \text{mA}$$

Assuming $I_{CQ} \cong I_{EQ}$ and letting $V_{CEQ} = 5$ V, we find

$$R_E = \frac{V^+ - V_{CEQ} - V^-}{I_{EQ}} = \frac{5 - 5 - (-5)}{0.255} = 19.6\ \text{k}\Omega$$

The term $(1 + \beta)R_E$ is

$$(1 + \beta)R_E = (101)(19.6) \Rightarrow 1.98\ \text{M}\Omega$$

With this large resistance, we can design a bias-stable circuit as defined in Chapter 3 and still have large values for bias resistances. Let

$$R_{TH} = (0.1)(1 + \beta)R_E = (0.1)(101)(19.6) = 198\ \text{k}\Omega$$

The base current is

$$I_B = \frac{V_{TH} - V_{BE}(\text{on}) - V^-}{R_{TH} + (1+\beta)R_E}$$

where

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5 = \frac{1}{R_1}(R_{TH})(10) - 5$$

We can then write

$$\frac{0.255}{100} = \frac{\frac{1}{R_1}(198)(10) - 5 - 0.7 - (-5)}{198 + (101)(19.6)}$$

We find $R_1 = 317\,\text{k}\Omega$ and $R_2 = 527\,\text{k}\Omega$.

Comment: The quiescent collector current $I_{CQ} = 0.255$ mA establishes the required r_π value which in turn establishes the required output resistance R_o.

Common-Base Amplifier

- Small-Signal Voltage Gain $(r_o = \infty)$

$$I_b = \frac{V_x}{r_\pi} \qquad V_x = -V_\pi$$

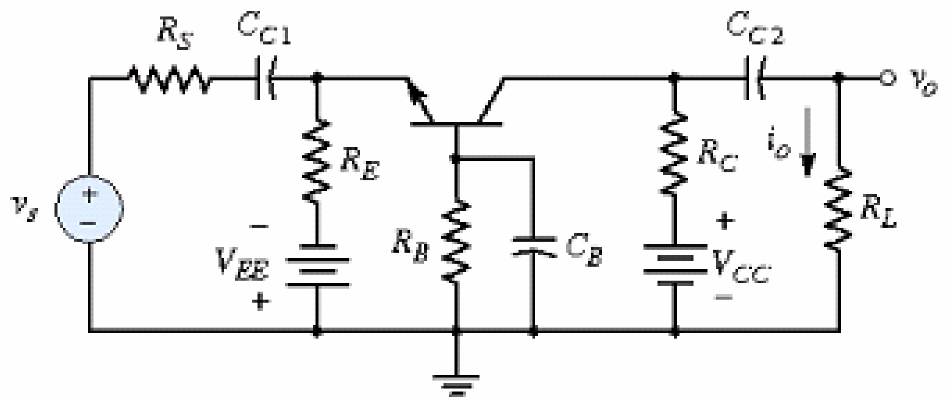
$$\frac{V_s - V_x}{R_s} = \frac{V_x}{R_E} + (1+\beta)\frac{V_x}{r_\pi}$$

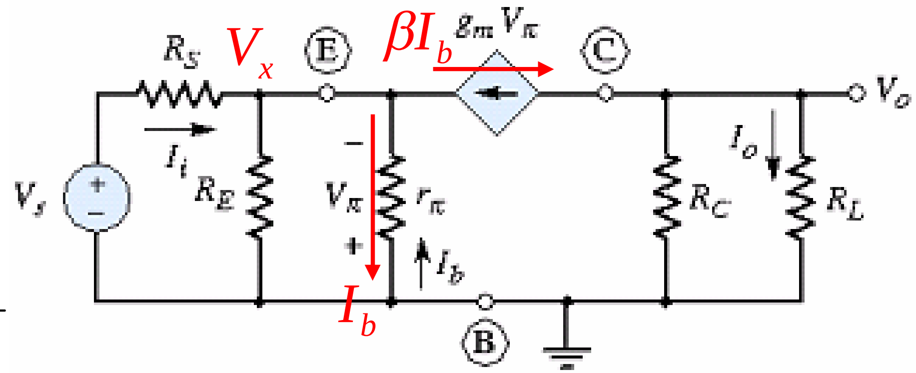
$$\frac{V_s}{R_s} = \left(\frac{1}{R_s} + \frac{1}{R_E} + \frac{1+\beta}{r_\pi}\right)V_x$$

$$V_x = \left(R_s // R_E // \frac{r_\pi}{1+\beta}\right)\frac{V_s}{R_s}$$

$$V_o = -g_m V_\pi \cdot (R_C // R_L)$$

$$= g_m (R_C // R_L)\left(R_s // R_E // \frac{r_\pi}{1+\beta}\right)\frac{V_s}{R_s}$$





$$A_v = \frac{g_m (R_C // R_L)}{R_s}\left(R_s // R_E // \frac{r_\pi}{1+\beta}\right) \approx g_m (R_C // R_L) \qquad (R_s \to 0)$$

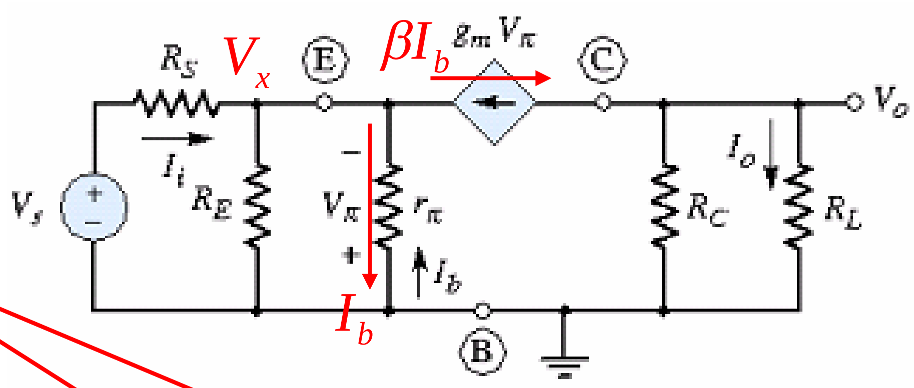
Common-Base Amplifier

- Small-Signal Current Gain

$$I_i = \frac{V_x}{R_E} + (1+\beta)\frac{V_x}{r_\pi}$$

$$= \left(\frac{1}{R_E} + \frac{\beta+1}{r_\pi}\right)V_x$$

$$= \frac{V_s}{R_E // (r_\pi / (\beta+1))}$$



$$V_x = (R_s // R_E // \frac{r_\pi}{1+\beta})\frac{V_s}{R_s} \approx V_s$$

as $R_s \to 0$

$$I_o = \frac{-g_m V_\pi R_C}{R_C + R_L} = \frac{g_m R_C}{R_C + R_L} V_s$$

$$A_i = \frac{I_o}{I_i} = \frac{g_m R_C}{R_C + R_L} \cdot \left[R_E // \frac{r_\pi}{1+\beta}\right]$$

$$R_E \to \infty, R_C >> R_L, A_i \approx \frac{\beta}{1+\beta} \to 1$$

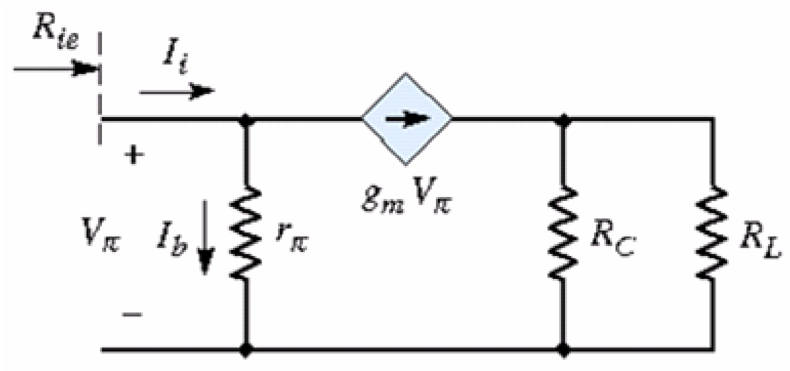
Common-Base Amplifier

- Input Impedance

$$I_i = (1+\beta)I_b$$

$$V_\pi = I_b r_\pi$$

$$R_{ie} = V_\pi / I_i = r_\pi /(1+\beta)$$



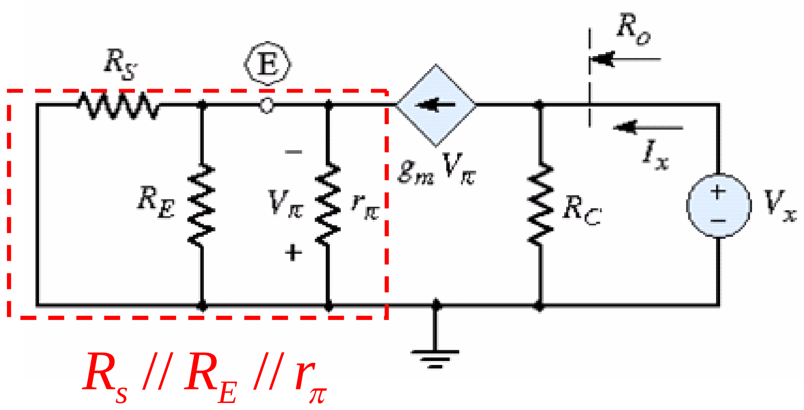
- Output Impedance

$$V_\pi = -(R_s // R_E // r_\pi) g_m V_\pi$$

$$[1+(R_s // R_E // r_\pi) g_m] V_\pi = 0$$

$$\Rightarrow V_\pi = 0$$

$$R_o = R_C$$



Multistage Amplifiers: Cascade Configuration

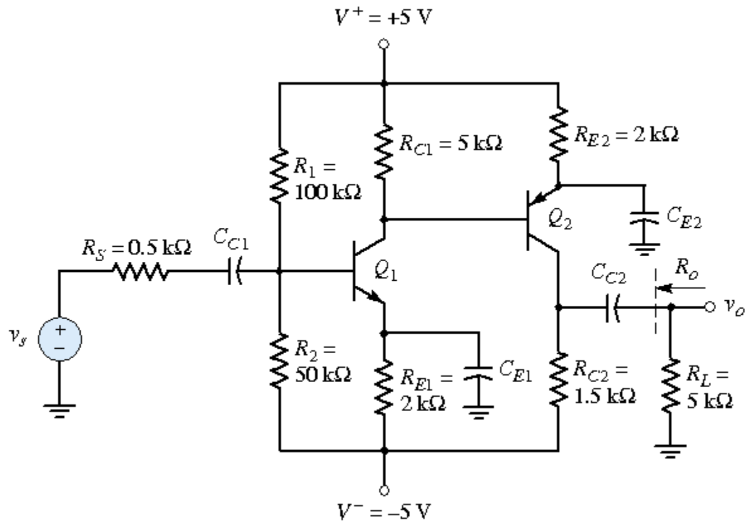


Figure 4.60 A two-stage amplifier in a cascade configuration

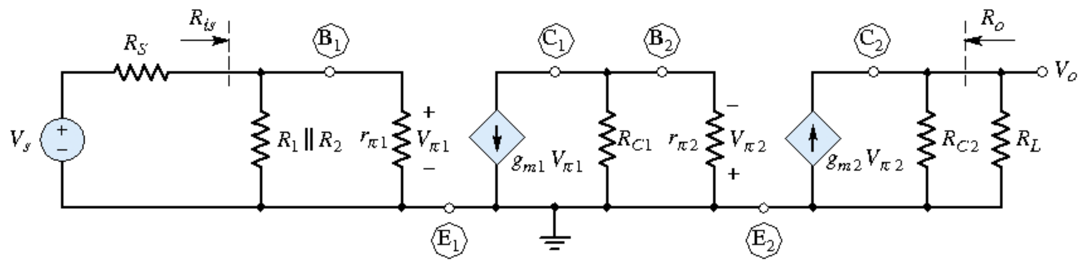


Figure 4.61 Small-signal equivalent circuit of the cascade configuration

$$A_v = \frac{V_o}{V_s} = g_{m1} g_{m2} (R_{C2} // R_L)(R_{C1} // r_{\pi2})\left(\frac{R_{is}}{R_s + R_{is}}\right) \qquad R_{is} = R_1 // R_2 // r_{\pi1}$$

Darlington Pair Configuration

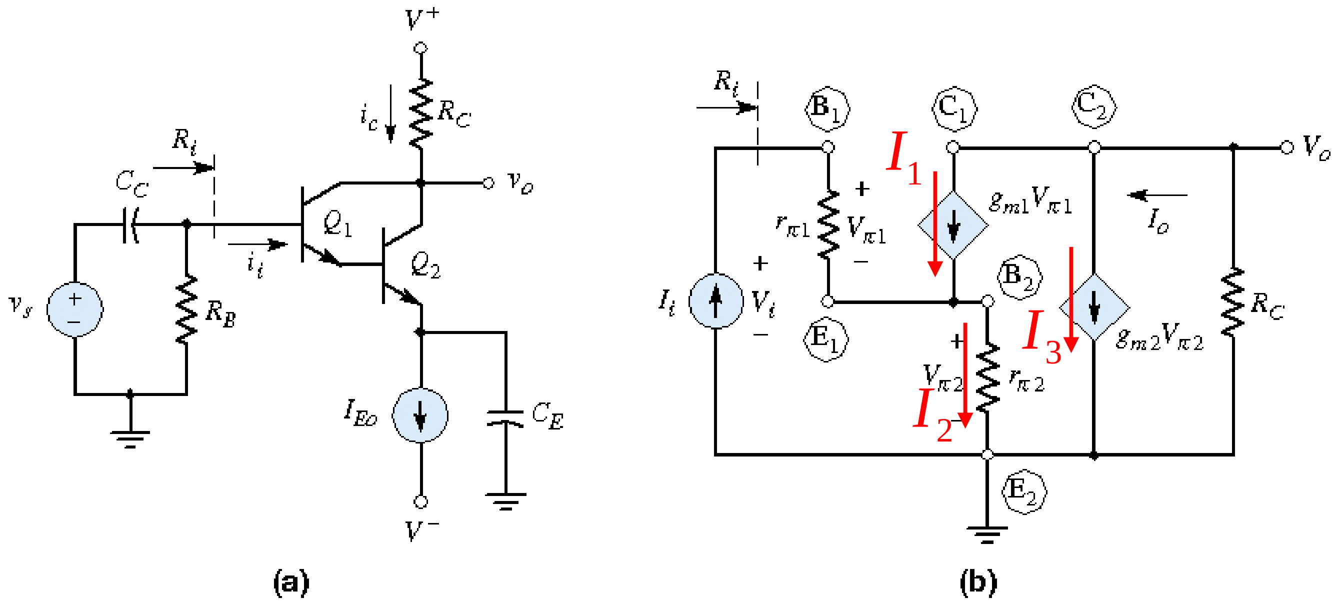


Figure 4.63 (a) A Darlington pair configuration; (b) small-signal equivalent circuit

$$I_1 = \beta_1 I_i$$

$$I_2 = (1+\beta_1) I_i$$

$$I_3 = \beta_2 I_2 = \beta_2 (1+\beta_1) I_i$$

$$I_o = I_1 + I_3 = (\beta_1\beta_2 + \beta_2 + \beta_1) I_i$$

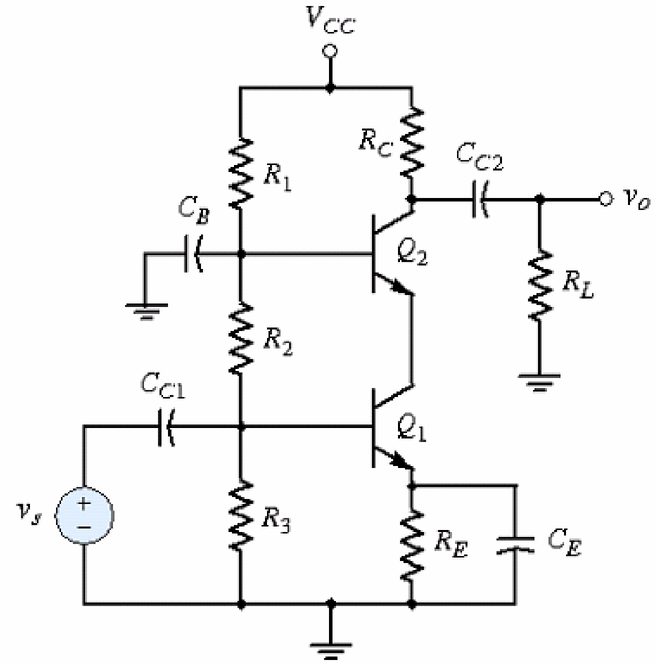
$$A_i = I_o / I_i = \beta_1\beta_2 + \beta_2 + \beta_1 \approx \beta_1\beta_2$$

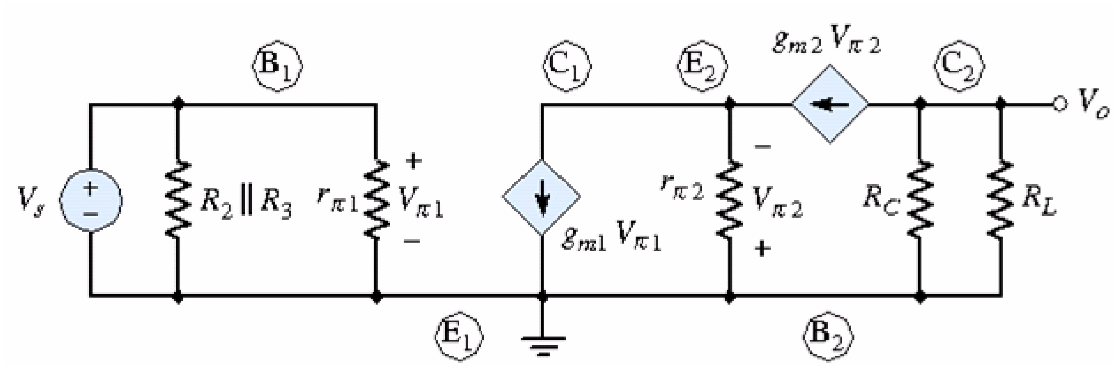
$$R_i = r_{\pi 1} + (1+\beta_1) r_{\pi 2}$$

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{CQ1}} = \frac{(\beta_1 + 1) V_T \cdot \beta_2}{I_{CQ2}} = (\beta_1 + 1) r_{\pi 2}$$

$$R_i = (\beta_1 + 1) r_{\pi 2} + (1+\beta_1) r_{\pi 2} = 2(\beta_1 + 1) r_{\pi 2}$$

Multistage Amplifiers: Cascode Configuration





$$V_{\pi 1} = V_s$$

$$g_{m1}V_{\pi 1} = \frac{V_{\pi 2}}{r_{\pi 2}} + g_{m2}V_{\pi 2}$$

$$V_{\pi 2} = \left(\frac{r_{\pi 2}}{1+\beta_2}\right)(g_{m1}V_s)$$

$$V_o = -(g_{m2}V_{\pi 2})(R_C \| R_L)$$

$$V_o = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C \| R_L)V_s$$

$$A_v = \frac{V_o}{V_s} = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C \| R_L)$$

$$g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right) = \frac{\beta_2}{1+\beta_2} \cong 1$$

$$A_v \cong -g_{m1}(R_C \| R_L)$$

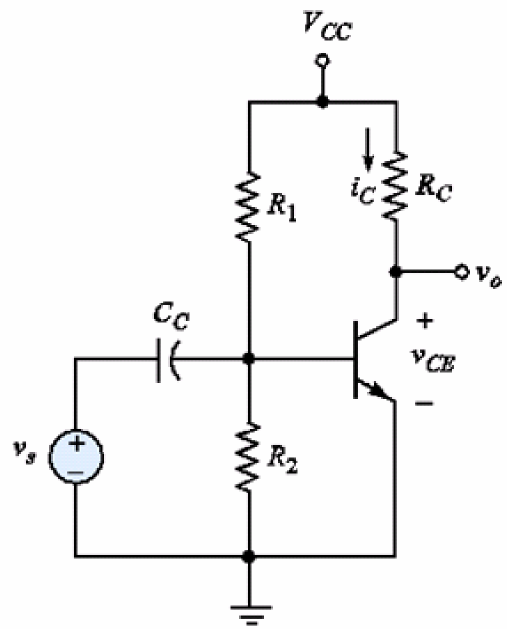
Power Consideration

- DC Power

$$P_{CC} = I_{CQ}V_{CC} + P_{\text{Bias}}$$

$$P_{RC} = I_{CQ}^2 R_c$$

$$P_Q = I_{CQ}V_{CEQ} + I_{BQ}V_{BEQ} \cong I_{CQ}V_{CEQ}$$



- Total Current and Voltage

$$v_s = V_p \cos \omega t$$

$$i_B = I_{BQ} + \frac{V_p}{r_\pi} \cos \omega t = I_{BQ} + I_b \cos \omega t$$

$$i_C = I_{CQ} + \beta I_b \cos \omega t = I_{CQ} + I_c \cos \omega t$$

$$v_{CE} = V_{CC} - i_C R_C = V_{CC} - (I_{CQ} + I_c \cos \omega t)R_C = V_{CEQ} - I_c R_C \cos \omega t$$

Power Consideration

- Total Power

$$\bar{p}_{cc} = \frac{1}{T}\int_0^T V_{CC} \cdot i_C \, dt + P_{\text{Bias}}$$

$$= \frac{1}{T}\int_0^T V_{CC} \cdot [I_{CQ} + I_c \cos\omega t] \, dt + P_{\text{Bias}}$$

$$= V_{CC} I_{CQ} + \frac{V_{CC} I_c}{T}\int_0^T \cos\omega t \, dt + P_{\text{Bias}}$$

(0)

$$= I_{CQ} V_{CC} + P_{\text{Bias}}$$

$$\bar{p}_Q = \frac{1}{T}\int_0^T i_C \cdot v_{CE} \, dt$$

$$= \frac{1}{T}\int_0^T [I_{CQ} + I_c \cos\omega t] \cdot [V_{CEQ} - I_c R_C \cos\omega t] \, dt$$

$$= I_{CQ} V_{CEQ} - \frac{I_c^2 R_C}{T}\int_0^T \cos^2\omega t \, dt$$

$$= I_{CQ} V_{CEQ} - \tfrac{1}{2} I_c^2 R_C$$

$$\bar{p}_{RC} = \frac{1}{T}\int_0^T i_C^2 R_C \, dt = \frac{R_C}{T}\int_0^T [I_{CQ} + I_c \cos\omega t]^2 dt$$

$$= \frac{I_{CQ}^2 R_C}{T}\int_0^T dt + \frac{2 I_{CQ} I_c}{T}\int_0^T \cos\omega t \, dt + \frac{I_c^2 R_C}{T}\int_0^T \cos^2\omega t \, dt$$

(0)

$$= I_{CQ}^2 R_C + \tfrac{1}{2} I_c^2 R_C$$