Electronics II, Exam-3, Spring 2021

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11th June, 2021, Prof. Dah-Chung Chang (E1-311)

Note: The scientific calculator is allowed in all Electronics II exams.

1. (35%) In the circuit shown in Fig. 1, the active load circuit is replaced by a current source in which the PNP transistors Q_2 and Q_3 are matched. The common-emitter current gain of transistors is denoted as β. Suppose that I_{REF} is obtained from another ideal current source.
   (a) Derive the exact relationship between i_{E1} and i_{C2}, and explain in what condition we have $i_{E1} \approx i_{C2}$. (10%)
   (b) To find the output resistance of the current source looking into the collector of Q_1, we may treat the emitter terminal of Q_1 as virtual ground in small-signal analysis for simplicity. Draw the small-signal equivalent circuit and write out the resistance looking into the base and collector of Q_3 from the emitter terminal of Q_1, and explain the reason. (10%)
   (c) Draw the small-signal equivalent circuit of the current source and show that the output resistance $R_{C1} \approx \beta r_{o1} / 2$, using the approximation obtained in (a) and (b). (10%)
   (d) Assume that β = 250 for all transistors, and that $V_{\text{AN}} = 150\text{V}$, $V_{\text{AP}} = 120\text{V}$, and $I_{\text{REF}} = 1\text{mA}$. Determine the small-signal voltage gain v_O / v_I. (5%)

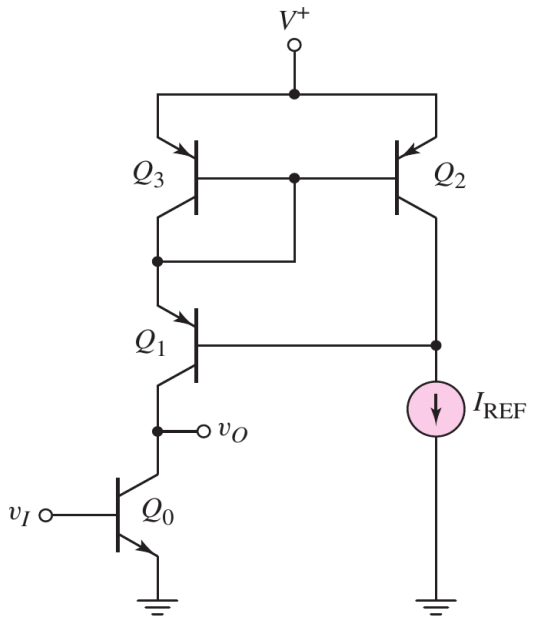

Fig. 1

2. (30%) The circuit in Fig. 2 is a two-transistor PMOS current mirror. Based on the reference current I_{REF}, we want to design the PMOS transistor M_3 and to evaluate the maximum output current I_O for a given load resistance *R*.

   (a) Write out the circuit equations that are required to obtain I_{REF}, and explain the reason why you construct those simultaneous equations and the processes how to solve for I_{REF}. (10%)

   (b) Assume that the circuit and transistor parameters of M_1 and M_2 are $V^+ = 3\text{V}$, $V^- = -3\text{V}$, $V_{TP1} = V_{TP2} = -1\text{V}$, $K_{p1} = 1\text{mA/V}^2$, and $K_{p2} = 9\text{mA/V}^2$. Suppose that $R = 12\text{k}\Omega$, determine the maximum value of I_O such that M_3 remains biased in the saturation region. (15%)

   (c) Determine the ratio parameters $(\text{W}/\text{L})_3$ of M_3 given that $k_p' = 0.1\text{mA}/\text{V}^2$ and $I_O = 0.2\text{mA}$. (5%)

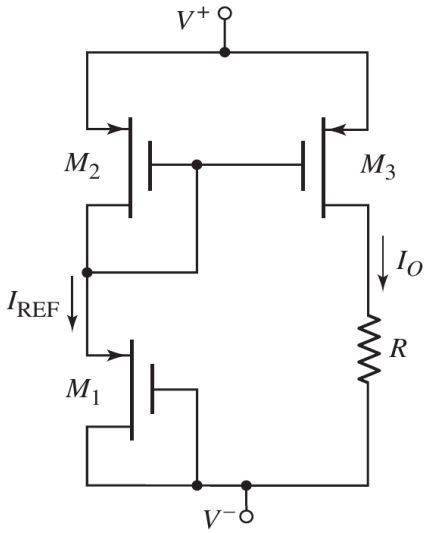

Fig. 2

3. (35%) Consider the multi-transistor current source in Fig. 3. Assume that M_1, M_2, and M_3 are identical except for their geometry ratios, and the circuit and transistor parameters are $V^+ = 5\text{V}$, $V_{TN} = 1\text{V}$, $k_n' = 80\mu\text{A/V}^2$, and $\lambda = 0$.
   (a) Let $I_{\text{REF}} = 0.1\text{mA}$ and the geometry ratio of M_3 be $(\text{W/L})_3 = 4$. Assume that M_1 and M_2 have the same W/L geometry ratio. Determine the ratio and explain how to use this assumption to obtain that value. (10%)
   (b) Suppose that the transistor parameters of M_4 is the same as M_1 except that $\lambda_4 = 0.05\text{V}^{-1}$. Determine the geometry ratio of M_4 for at least $I_{O1} = 0.5\text{mA}$ as M_4 remains biased in the saturation region. (10%)
   (c) Assume that the transistor parameters of M_5 is the same as M_1 except that $\lambda_5 = 0.01\text{V}^{-1}$. What is the maximum value of R_S for $I_{O2} = 40\mu\text{A}$? (5%)
   (d) Let $R_S = 10\text{k}\Omega$. Determine the geometry ratio of M_5 for at least $I_{O2} = 40\mu\text{A}$ as M_5 remains biased in the saturation region, and determine the output resistance R_{D5} looking into the drain terminal of M_5. (10%)

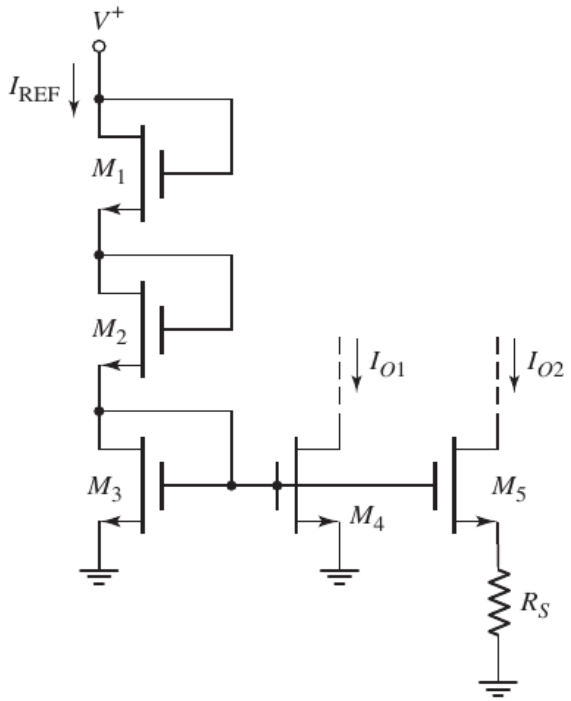

Fig. 3