Electronics II, Exam-4, Spring 2021

Department of Communication Engineering, National Central University

25th June, 2021, Prof. Dah-Chung Chang (E1-311)

Note: The scientific calculator is allowed in all Electronics II exams.

1. (20%) Suppose that the capacitor C_E in Fig.1 is short in the analysis of small-signal equivalent circuit. Derive the expression of the differential-mode output resistance R_O looking from v_O in terms of transistors' small-signal parameters such as $g_{m1}, g_{m2}, \ldots, r_{\pi 1}, r_{\pi 2}, \ldots, \beta_1, \beta_2, \ldots, r_{o1}, r_{o2}, \ldots, r_{o6}$ and the resistances as shown in Fig.1. (about 3-4% for backward pursuing each transistor)

   Note: You need to write out complete analysis processes for every steps with sketching necessary small-signal equivalent circuit for explanation)

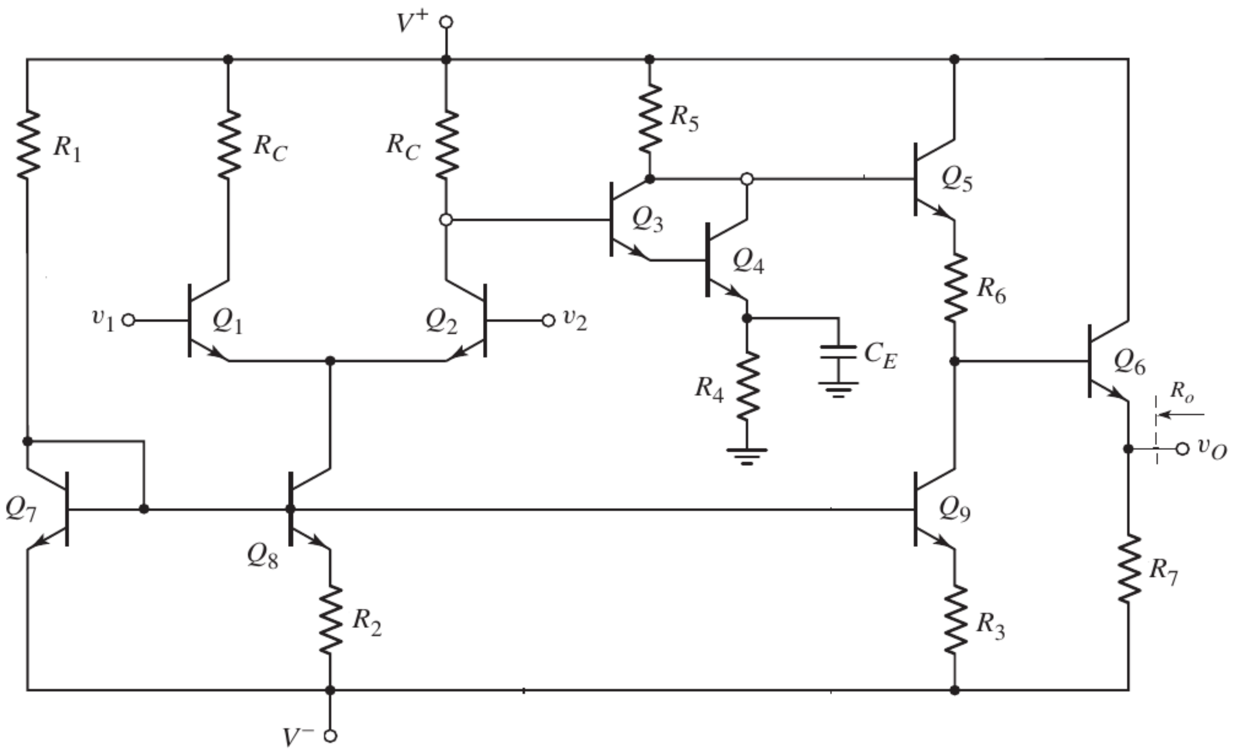

Fig. 1

2. (40%) The transistor parameters for the circuit in Fig. 2 are that

M_1 and M_2: $K_n = 0.2\ \text{mA/V}^2$, $V_{TN} = 0.8\ \text{V}$, and $\lambda = 0$;

Q_3 and Q_4: $V_{BE(\text{on})} = 0.7\ \text{V}$, $V_{CE(\text{sat})} = 0.2\ \text{V}$, $\beta = 250$, $V_{A3} = \infty$, and $V_{A4} = 90\ \text{V}$.

Suppose that the output resistance of the current source is $R_o = 200\ \text{k}\Omega$. Design the circuit such that $v_{O2} = 2\ \text{V}$, $I_{C3} = 0.25\ \text{mA}$, and $I_{C4} = 2\ \text{mA}$.

(a) Determine the maximum value of the common-mode input voltage for v_1 and v_2. (5%)

(b) Determine R_1 and R_2 if we make v_O as close to zero as possible. (5%)

(c) Sketching the small-signal equivalent circuit, derive the expression of the voltage gain v_O / v_{O2} and determine the value. (10%)

(d) Sketching the small-signal equivalent circuit, derive the expression of the common-mode voltage gain $A_{cm1} = v_{O2} / v_1$. (10%)

(e) Determine the value of the overall CMRR_{dB}. (5%)

(f) Determine the output resistance looking from v_O. (5%)

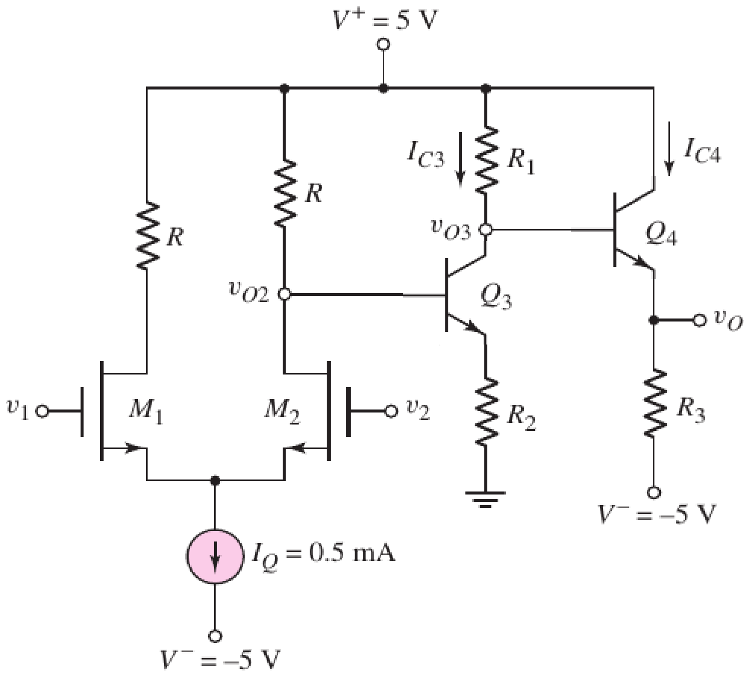

Fig. 2

3. (40%) The differential amplifier in Fig. 3(a) has a pair of NMOS transistors M_3 and M_4 as input devices, a pair of PMOS transistors M_1 and M_2 as an active load in a current mirror configuration, and a pair of NMOS transistors M_5 and M_6 connected as the current source biased with I_Q. Assume that all transistor characteristics are identical, that is, $K_n = K_p$, $\lambda_n = \lambda_p$, and $V_{TP} = -V_{TN}$. Let g_m and r_o denote the transconductance and output resistance of M_1, respectively. Because the active load circuit is not symmetrical, we can consider the small-signal equivalent half-circuit as split in Fig. 3(b) and let $i_d \approx Gv_1$. Follow the next steps to analyze the differential-mode gain, common-mode gain, and CMRR.

   (a) Sketching the small-signal equivalent circuit, determine the equivalent resistance R_{im} looking into the drain terminal of M_1. (5%)

   (b) Considering the case of $v_1 = -v_2 = v_d / 2$ for the differential mode, what are R_o, Gv_2, V_{sg2}, R_{om}, and the differential-mode voltage gain $A_d = v_O / v_d$. (10%)

   (c) Considering the case of $v_1 = v_2 = v_{cm}$ for the common mode, show that the Norton equivalent circuit model looking into the drain terminal of M_4 is $R_o \approx g_m r_o^2$ and $Gv_2 \approx v_{cm} / r_o$. (10%)

   (d) Sketching the small-signal equivalent circuit, derive the expression of the common-mode voltage gain $A_{cm} = v_O / v_{cm}$ with the approximation $1 - g_m\left(\frac{1}{g_m} \| r_o\right) \approx \frac{1}{g_m r_o}$. (10%)

   (e) Derive the approximate expression of CMRR in terms of K_n, λ_n, and I_Q. (5%)

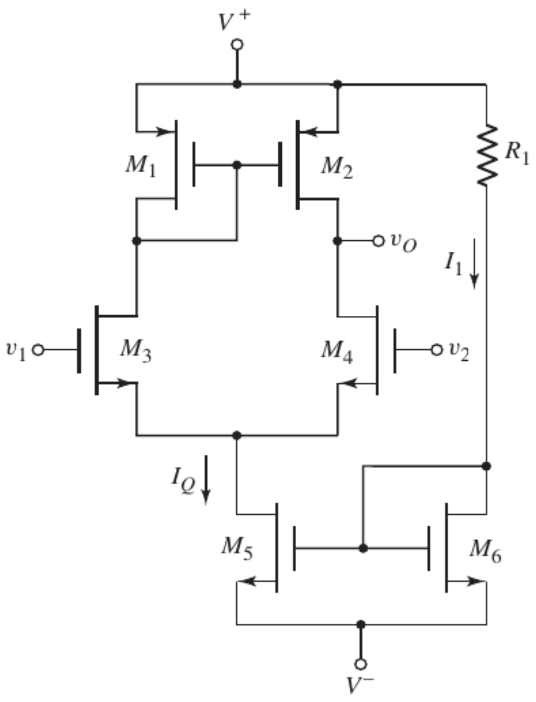

Fig. 3(a)

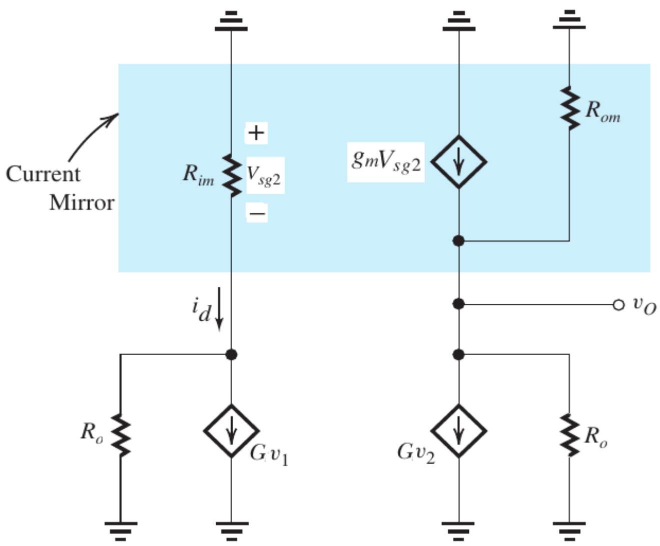

Fig. 3(b)