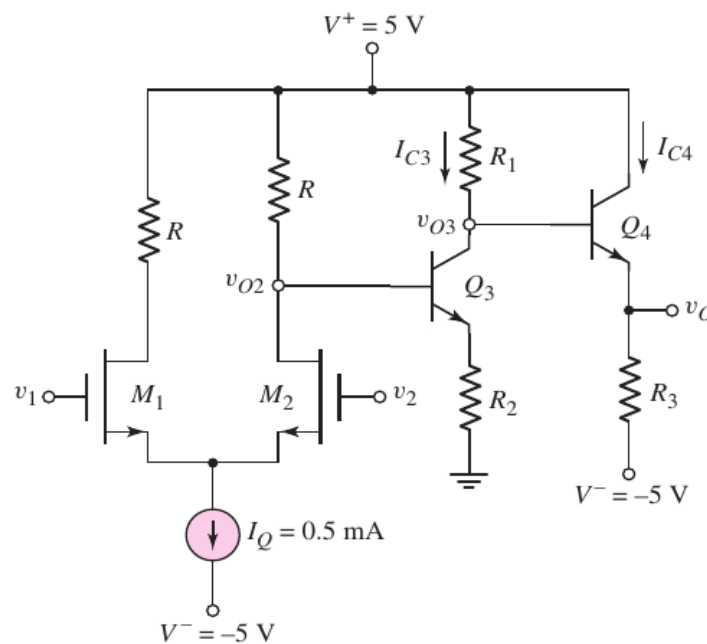
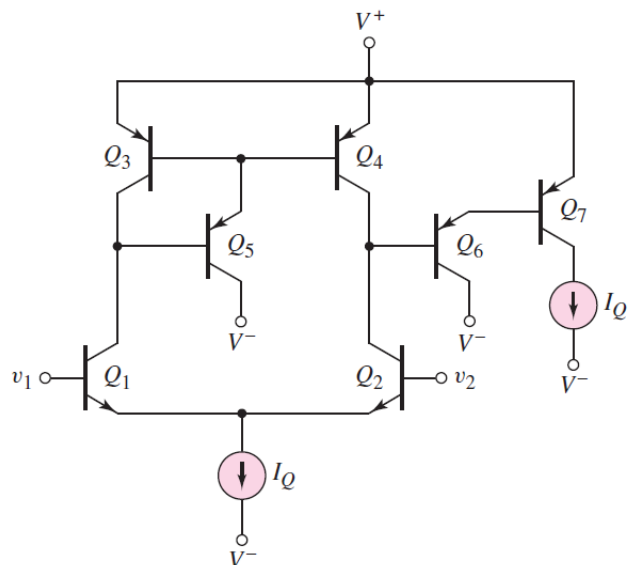


**Electronics II, Exam-4, Spring 2022**  
 Department of Communication Engineering, National Central University  
 June 17, 2022, Dr. Dah-Chung Chang (E1-311)

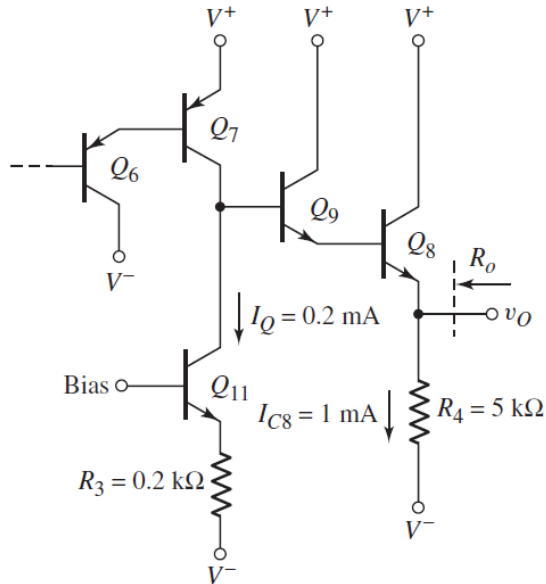
1. (30%) Suppose that the output resistance of the current source is  $R_o$ , the transconductance of the MOS transistors is  $g_m$ , and the common-emitter current gain of the BJT transistors is  $\beta$ .
- (a) Sketch the small-signal equivalent circuit and derive the expression of the voltage gain  $v_o/v_{o2}$ . (10%)
  - (b) Sketch the small-signal equivalent circuit and derive the expression of the common-mode voltage gain  $A_{cm1} = v_{o2}/v_1$ . (10%)
  - (c) Derive the overall  $CMRR_{dB}$ . (5%)
  - (d) Sketch the small-signal equivalent circuit and derive the output resistance looking from  $v_o$ . (5%)



2. (15%) The diff-amp has a three-transistor active load circuit and a Darlington pair configuration connected to the output. Determine the bias current  $I_{Q1}$  in terms of  $I_Q$  such that the diff-amp dc currents are balanced.



3. (20%) The output stage is a Darlington pair emitter-follower configuration. Assume  $\beta = 120$  for all npn transistors and  $\beta = 90$  for all pnp transistors. Let  $V_{A7} = 60 \text{ V}$  for  $Q_7$ ,  $V_{A11} = 120 \text{ V}$  for  $Q_{11}$ , and  $V_A = \infty$  for all other transistors. Determine the output resistance  $R_o$ .



4. (35%) Consider the following BJT operational amplifier circuit, in which the transistor parameters are:  $\beta = 120$ ,  $V_{BE(\text{on})} = 0.7 \text{ V}$  (except for  $Q_8$  and  $Q_9$ ), and  $V_A = \infty$ . We have  $I_Q = 0.4 \text{ mA}$ .

- Find the dc output voltage  $V_o$ . (10%)
- Find the input resistances  $R_{i2}$  and  $R_{i3}$ . (10%)
- Determine the overall differential-mode voltage gain  $A_d = v_o / (v_1 - v_2)$ . (15%)

