Electronics II, Exam-3, Spring 2025

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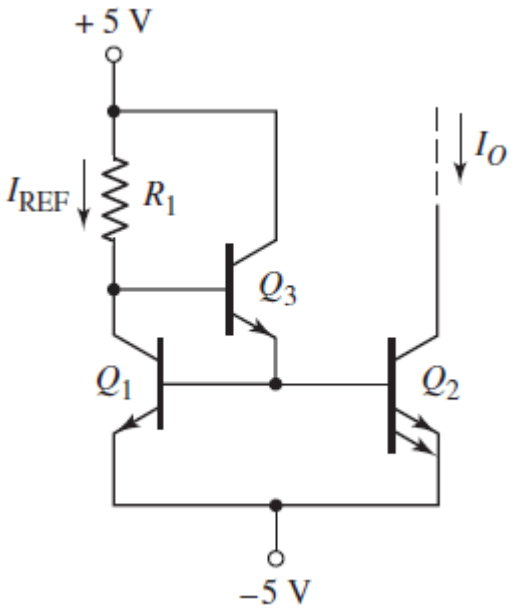
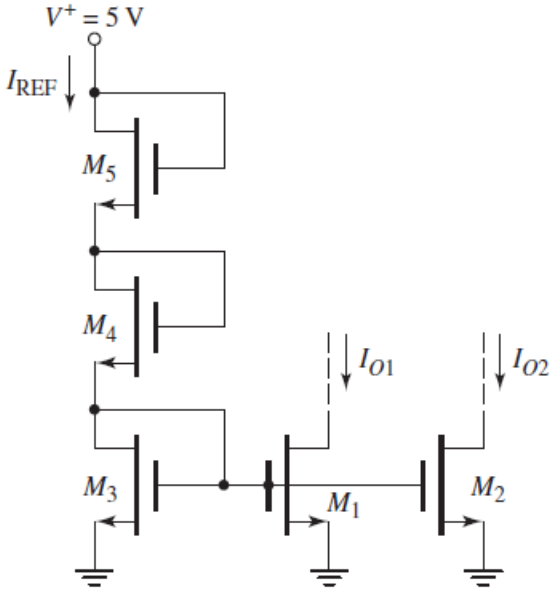
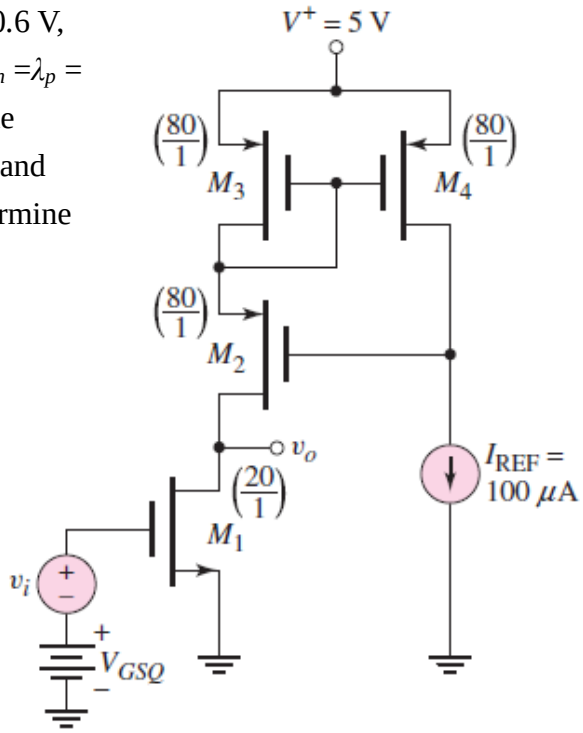
1. (20%) The transistor parameters for Q_1 and Q_2 are $V_{BE1,2}(\text{on}) = 0.7\text{V}$ and $\beta_{1,2} = 90$. The parameters for Q_3 are $V_{BE3}(\text{on}) = 0.6\text{V}$ and $\beta_3 = 60$. Assume $V_A = \infty$ for all transistors. Find the resistance R_1 such that $I_O = 0.5\,\text{mA}$.



2. (20%) Assume M_3, M_4, and M_5 are identical, and the transistor parameters are $V_{TN} = 0.7\text{V}$, $k_n' = 80\mu\text{A}/\text{V}^2$, and $\lambda_n = 0$. Design the NMOS circuit for their (W/L) ratios such that $I_{REF} = 0.1mA$, $I_{O1} = 0.2mA$, and $I_{O2} = 0.3mA$.



3. (30%) The parameters of the transistors are V_{TN} = 0.6 V, V_{TP} = −0.6 V, k_n' =100μA/V^2, k_p' = 60μA/V^2, and λ_n =λ_p = 0.02V^{-1}. The width-to-length ratios are shown in the figure. The value of V_{GSQ} is such that I_{D1} = 100μA, and M_1 and M_2 are biased in the saturation region. Determine the small-signal voltage gain $A_v = v_o/v_i$.



4. (30%) The NMOS transistor parameters are $V_{TN} = 0.4\text{V}$, $k_n' = 100\mu\text{A/V}^2$, $\lambda_n = 0$ and the PMOS transistor parameters are $V_{TP} = -0.6\text{V}$, $k_p' = 40\mu\text{A/V}^2$, $\lambda_p = 0$. Design the circuit such that $I_{REF} = 50\mu A$, $I_{O1} = 0.12mA$, $I_{D3} = 25\mu A$, $I_{O2} = 0.15mA$, $V_{SD2}(\text{sat}) = 0.35\text{V}$, and $V_{DS5}(\text{sat}) = 0.35\text{V}$.